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Phoenix Model 5500A

Telecommunications Analyzer

Test Smart . . . Test Phoenix

34-00057-5.01

Phoenix Microsystems,
A DIVISION OF CTC
991 Discovery Drive
Huntsville, AL 35806
(205) 922–1200 • 1–800 866–8480 • FAX (205) 922–1256

Preface

About This Manual

This manual is arranged so you can quickly and easily find the information you need. The following is an overview of the contents of this manual.

- Chapter 1, General, familiarizes you with general 5500A highlights and explains how to unpack your test set properly.
- Chapter 2, Overview, describes the 5500A controls, indicators, and connectors. The test set operation overview is also included.
- Chapter 3, Operation, tells you how to use the 5500A for common communication systems tests.
- Chapter 4, Parameter Descriptions, describes menu parameters displayed on the 5500A test set.
- Chapter 5, Remote/Printer Operation, explains remote operation from a terminal and printer operation.
- Chapter 6, Performance Monitoring, defines G.821 parameters.
- Chapter 7, Maintenance, includes all maintenance/calibration procedures required for the 5500A test set.
- Chapter 8, Options, provides a brief explanation of modules available for use with the 5500A test set.
- Appendices
  A Model 5500A Specifications.
- NOTE – provides additional information.
- CAUTION – alerts you to situations where you could cause possible damage to the 5500A or the circuit under test.
- WARNING – alerts you to situations that could cause personal injury.

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Reorder Number 34–00057

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Warranty

Phoenix Microsystems warrants each 5500A against defects in material and workmanship for a period of two years (options are warranted for one year) from the date the 5500A was shipped to the customer. If at any time during the warranty period, the 5500A should malfunction, Phoenix will repair, or at Phoenix's option, replace the unit free of charge. The remedies listed herein are the users sole and exclusive remedies. Phoenix shall not be liable for any indirect, direct, incidental, or consequential damages. Owner must return the unit to the factory, shipping prepaid and packaged to best commercial standard for electronic equipment. Phoenix will pay shipping charges for delivery on return. Customer is responsible for mode and cost of shipment to Phoenix.

Warranty does not apply if the unit has been damaged by accident, misuse or as a result of service or modification by other than Phoenix personnel.

Safety Summary

The following safety precautions must be observed whenever the 5500A is operated, serviced, or repaired. Failure to comply with these and other specific warnings and cautions within this instruction book is a violation of Phoenix Microsystems' safety standards of design, manufacture, and intended use of the test set. Phoenix assumes no liability for the customer's or user's failure to comply with these precautions.

Grounding – The 5500A chassis and cabinet must be connected to an electrical ground for proper operation and to minimize shock hazard. The unit is furnished with a three conductor ac power cable which incorporates a ground lead. The power cable must be connected to an approved three contact electrical outlet or to a three conductor to two conductor adapter with a grounding wire (green) connected to electrical ground at the outlet.

Explosive Atmosphere – The 5500A must never be operated in the presence of any flammable gases or fumes. Power must not be applied to this or any instrument under such conditions due to the potential for explosion.

High Voltage Circuits – Only qualified maintenance personnel should remove the instruments covers. Dangerous voltages may exist within the unit even after the power cable has been disconnected. Do not attempt to replace components with the power cable connected.

Line Voltage – Before connecting the ac power cord make sure that the line voltage switch on the 5500A power supply module is set to match the source voltage.

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General

1.0 INTRODUCTION

This section of the manual contains general information about the Model 5500A Telecommunications Analyzer. Included are design highlights, theory of operation, a list of provided equipment, and general servicing information.

1.1 DESIGN HIGHLIGHTS

The 5500A is capable of bit error rate testing and system analysis on U.S.A. and international communications links operating from 50bps to 13Mbps. The 5500A is equipped with software driven menus and the ability to store test setups in memory. Design highlights of the 5500A include:

- Fractional (Nx64) testing capabilities
- Plug–in interfaces permit testing to international standards
- DDS testing at the DS0 (64 kbps) level
- Digital frequency synthesizer with 1ppm accuracy and .1 Hz resolution from 50 Hz to 500 kHz, 1Hz resolution from 500 kHz to 6.5 MHz, and 2 Hz resolution from 6.5 MHz to 13MHz
- RS–232 and IEEE–488 interfaces for remote control
- Tests T1 framed, SLC®96, unframed, and ESF formats
- User programmable test setup permits two button automatic setup and testing
- Allows BERT stress testing with patterns trapped from "Live" traffic to locate pattern sensitive problems
- Jitter injection and measurement at 1.544 and 2.048Mbps
- Simultaneous bit, frame, logic, and bipolar violation measurements
- 64K bit trap for bit–by–bit analysis of data stream

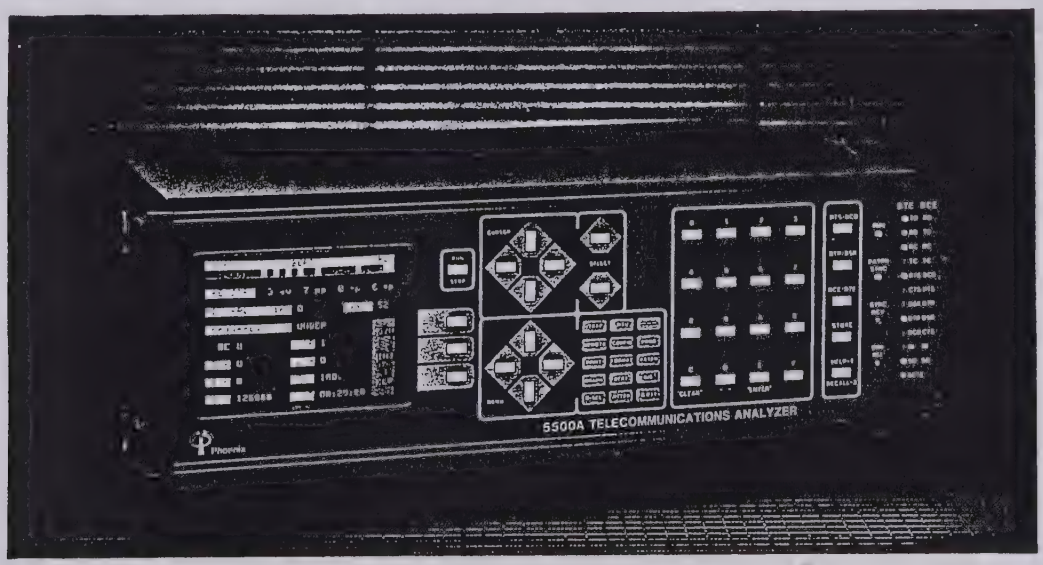

Figure 1–1. Model 5500A Test Set.

1.2 THEORY OF OPERATION

The 5500A is the most powerful and versatile data communications analyzer in its class. It is an internationally approved instrument designed for error and performance analysis of telecommunications systems operating at 50 bps to 13 Mbps. The test set is packaged in a rugged, aluminum case, with convenient handles and flip down feet for easy viewing of the display. The 5500A may be used as a mobile test set or may be rack–mounted for stationary use.

The 5500A is a menu driven test set with two bidirectional keys to control menu selection and cursor movement. Softkey functions are provided to control parameter functions to the selected menu. The hexidecimal keypad permits direct entry of user patterns, synthesizer frequency, and other BERT information. Front panel LEDs indicate the status of key DTE/DCE lines to low speed data interface modules.

Some of the main features of the 5500A are a 64k bit data trap, frequency synthesizer, network loop delay measurement, event timing and full remote testing capabilities via RS–232 and IEEE ports. Also there is a wide selection of test patterns and four user programmable patterns. The 5500A provides ten user defined test setups for instantaneous testing. A five inch, high resolution CRT provides numerical and/or graphic display of test results.

There are a full range of plug–in interface modules that permit testing of U.S. and International standards. The 5500A has been designed to grow as the needs of the industry continue to grow. These modules coupled with menu driven software, permit the 5500A to be continually updated to keep abreast of current technology. For test requirements ranging from T1 span analysis to LAN management to digital transmission service/switching, the 5500A provides the latest test capabilities for today and tomorrow.

1.3 EQUIPMENT SUPPLIED

Table 1–1 presents the options and accessories provided with the 5500A test set.

1.4 TOOLS AND TEST EQUIPMENT

The 5500A is a full function test set requiring no additional test equipment or tools to perform a test. The following optional equipment may be used with the 5500A.

1. Printer (RS–232 interface). The 5500A is compatible with any serial 80–column printer. Recommended printers include the Citizen 200 GX dot matrix printer or the Brother M–1109 Impact dot matrix printer.

Table 1–1. Model 5500A Equipment.

EQUIPMENT	QUANTITY	DESCRIPTION
F–5500–100A–11111	1	Communication Analyzer, 110V, 60 Hz
F–5501A–057–1	1	Cable, RS–449 to EIA–530
7–5501–200–1	2	Cable, RS–232, M–M/F, 5 ft.
7–5501–400–1	1	Cable, RS–449, M–M/F, 5 ft.
33–00085	1	Cable, Bantam to Bantam, red, 6 ft.
33–00086	1	Cable, Bantam to Bantam, black, 6 ft.
33–00089	1	Cable, Bantam to 310, red, 6 ft.
33–00090	1	Cable, Bantam to 310, black, 6 ft.
33–00160	1	Power Cord, 110V
18–00112	1	Adjustment Trimmer Tool
34–00057	2	Manual

1.5 INTERFACE OPTIONS

The Options section of this manual presents a complete listing and a brief description of the interface modules that are available for use with the 5500A.

1.6 MANUAL

This manual contains information required to install, check, and operate the 5500A test set. The following sections are included.

General
Overview
Operation
Parameter Descriptions
Remote/Printer Operation
Performance Monitoring
Maintenance
Options
Appendix A – Specifications

1.7 UNPACKING AND INSPECTION

The 5500A is carefully packaged to prevent damage in shipment. Upon receipt carefully inspect the condition of the shipping container. If the container shows any evidence of damage, notify the carrier before continuing with the unpacking. **Failure to notify the carrier of damage may negate your future claims for damages.** After unpacking, examine the exterior of the unit to insure it is free of scratches, dents, and any other visible sign of damage. If the 5500A was damaged in shipment, file a claim with the carrier immediately. Check to ensure you have received the supplied equipment (listed in paragraph 1.2 of this manual).

1.8 SERVICE AND ADJUSTMENT

1.8.1 Cathode Ray Tube (CRT)

Use caution when handling the CRT. To avoid breakage of the CRT and the resulting implosion, do not handle the 5500A in a rough manner while the internal circuitry is exposed. Removal, repair, or replacement of the CRT should only be done by qualified maintenance personnel.

1.8.2 Fuses

Always replace a blown fuse with an identical replacement fuse. Never use a fuse of a larger value or attempt to defeat or bypass the fuse.

1.8.3 Environmental

Do not exceed the operating temperature limits (0 to 50° C).

1.8.4 Interface Modules

Do not apply power to the 5500A without an interface module plugged into the unit. Never remove an interface module from or insert an interface module into the 5500A while the power is on. Always remove power first to prevent possible damage to the interface module and/or the 5500A.

1.9 CUSTOMER HOT LINE

Phoenix has established a customer hot line to provide our customers 24–hour, 7–day–a–week technical support. If you are experiencing any technical difficulties with your 5500A, please call 1–800–866–8480, extension 255.

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Chapter 2 – Overview

2.0 INTRODUCTION

This section of the manual contains a general overview of menus and operating procedures for the Model 5500A Bit Error Rate Test Set. Power–up and setup instructions are also included. (Some menus are interface module dependent.)

2.1 CONTROLS AND INDICATORS

Table 2–1 presents 5500A front panel controls and indicators. Table 2–1 is keyed to Figure 2–1. Table 2–2 presents the rear panel controls and connectors and is keyed to Figure 2–2.

Table 2–1. Model 5500A Front Panel Controls and Indicators.

INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
1		RUN/STOP	Controls 5500A operation. RUN LED will be on when 5500A is in the RUN mode.
2	TRAP MSU — REMOTE CONFIG PROG PRINT FORMAT PATRN GRAPH BERT BIG G–SEL JITTER G.821	There is no mnemonic for the menu layout.	Provides a visual aid to the location of the various menus contained in the 5500A menu matrix.
3		CURSOR	These four keys move the cursor. The cursor moves in the direction indicated by the arrow surrounding the key. The keys "wrap–around". Pressing the up key, for example, moves the cursor to the top most position and then in the lower most position.

Table 2–1. Model 5500A Front Panel Controls and Indicators (Cont.).

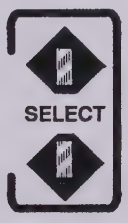
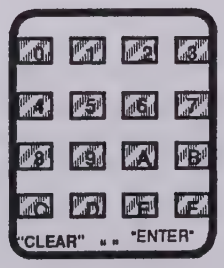
INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
4		SELECT	After positioning the cursor over the desired parameter, the SELECT keys are used to scroll through (up/down) parameter values.
5		MENU	These four keys are used to move around the matrix of menus to bring the desired menu to the screen. These keys do not "wrap–around". If you have reached the limit of travel for a key, pressing that key will cause an audio tone to sound and the display will not change.
6		The mnemonic for the three "softkeys" is software controlled and varies with each menu.	These three keys are referred to as "softkeys". Their function varies with the menu that is present on the CRT. The function of these softkeys is explained in the menu descriptions.
7		There is no mnemonic for the keypad.	The hexidecimal keypad is used to enter data (ie., user patterns, menu selection, user program names, and etc.) required for particular operations. When setting a Bit Rate, the **C** key is used as a clear key, the **D** key to enter a decimal point, and the **E** key to enter a frequency.

Table 2–1. Model 5500A Front Panel Controls and Indicators (Cont.).

INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
8	RUN ●	RUN	This yellow LED is illuminated when the 5500A is in the run mode. When in RUN, data is accumulated on the incoming bit stream. When stopped, the 5500A transmitter is still running, but results are not tabulated on received data.
9	PATRN SYNC ●	PATRN SYNC	This yellow LED is illuminated when the 5500A is in pattern synchronization with the incoming data stream.
10	SYNC REC ●	SYNC REC	This yellow LED is illuminated when the 5500A has recovered synchronization after having lost synchronization due to errors in the incoming data.
11	ERR INJ ●	ERR INJ	This yellow LED is illuminated whenever errors are being injected by the 5500A into the outgoing (transmit) data stream.
12		RTS/DCD	Toggles RTS in the DTE mode and DCD in the DCE mode.
		DTR/DSR	Toggles DTR in the DTE mode and DSR in the DCE mode.
		DCE/DTE	Selects DCE or DTE mode for the interface module.
		STORE	Stores current test setup in selected memory location for recall.
		HELP–1	Selects HELP menu (press once) or recalls a previously stored test setup from memory (press twice).
		RECALL–2	

Table 2–1. Model 5500A Front Panel Controls and Indicators (Cont.).

INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
13	DTE / DCE • TD (Transmit Data) / RD • RD (Receive Data) / TD • RC (Receive Clock) / RC • TC (Transmit Clock) / TC • RTS (Request to Send) / DCD • CTS (Clear to Sends) / RTS • DSR (Data Set Ready) / DTR • DTR (Data Terminal Ready) / DSR • DCD (Data Carrier Detect) / CTS • RI (Ring Indicator) / RI • SQ (Signal Quality) / SQ • SCTE (Transmit Clock Internal)	No mnemonic is assigned to the interface activity indicators.	These LEDs monitor the status of the interface connector lines and therefore are dependent upon the interface module installed.

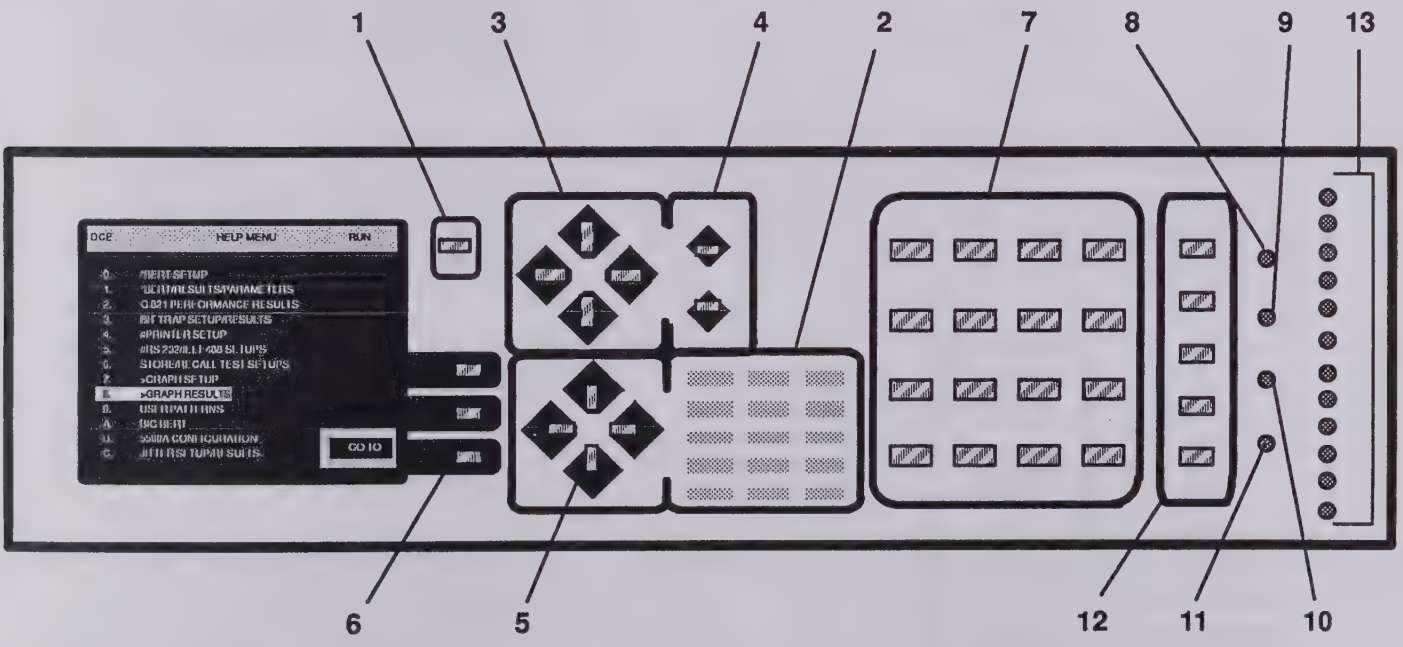


Figure 2–1. Model 5500A Front Panel Controls and Indicators.

Table 2–2. Model 5500A Rear and Bottom Panel Controls and Indicators.

INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
1			Power cord connector for 5500A. Before connecting main power be sure unit is set to match local power (refer to paragraph 2.12).
2			Main power fuse for 5500A. A 3 amp, 250 volt, fast blow mini fuse. Always replace with a fuse of an identical current and voltage rating.
3			Main power switch for the 5500A. The 1 position is "ON" and the 0 position is "OFF". Power on is also indicated by CRT illumination. Power is 47–440 cycles, 2.5A, 100–240 VAC.
4			The following 10 test points provide several of the internal 5500A signals to the user. These signals may be used for any purpose. One of the common uses is to provide a trigger signal for an oscilloscope. These signals are all applied to the rear panel through TTL buffers.
		TXD	Transmit data (transmitted by the 5500A).
		TXC	Transmit clock.
		XMIT PAT	Transmit pattern. A pulse that is synchronous with the beginning of the pattern and at the same repetition rate as the pattern.
		ERR	Error injection. A pulse each time an error is injected into the transmit data stream.

Table 2–2. Model 5500A Rear and Bottom Panel Controls and Indicators (Cont.).

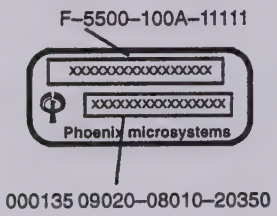
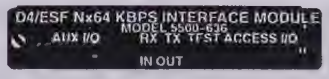
INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
4 (cont.)		SP	Spare. Not Used.
		RXD	Receive data (received by the 5500A).
		RC	Receive clock.
		REC PAT	Receive pattern sync. A pulse that is synchronous with the start of the pseudorandom receive pattern and is at the receive pattern repetition rate.
		REC SYNC	Recovered Sync. A pulse each time the 5500A recovers sync.
		GND	Signal Ground.
5		RS–232	RS–232 interface port for connection of a printer for printing data/graphs or connection of a terminal for remote control operation.
6		IEEE–488	IEEE–488 interface port for connection of a controller for remote control operation.
7		EXT TRIGGER	BNC connection provided for an external device to set a trigger point for the data bit trap function.
8			Identification plate contains model number (F–5500–100A –11111), serial number (000135 09020–08010–20350). The remaining digits represent internal manufacturing codes.

Table 2–2. Model 5500A Rear and Bottom Panel Controls and Indicators (Cont.).

INDEX	CONTROL INDICATOR	MNEMONIC	FUNCTION
9			Interface module which provides conversion between user protocol and internal TTL logic used by the 5500A. Instructions for the installed/ purchased options are located in the applicable option manual.
10		USER CLK	The user may connect an external clock to this input connector. All functions of the 5500A will then be slaved to this external clock when external clock is selected on the setup menu. This is not applicable to T1 or E1 modules.
11		VIDEO	RS–170 composite video available at this jack to provide a video signal to an external monitor if desired.
12		BRIGHTNESS	Control to adjust the intensity of the front panel CRT. This control is located on the bottom panel of the test set.

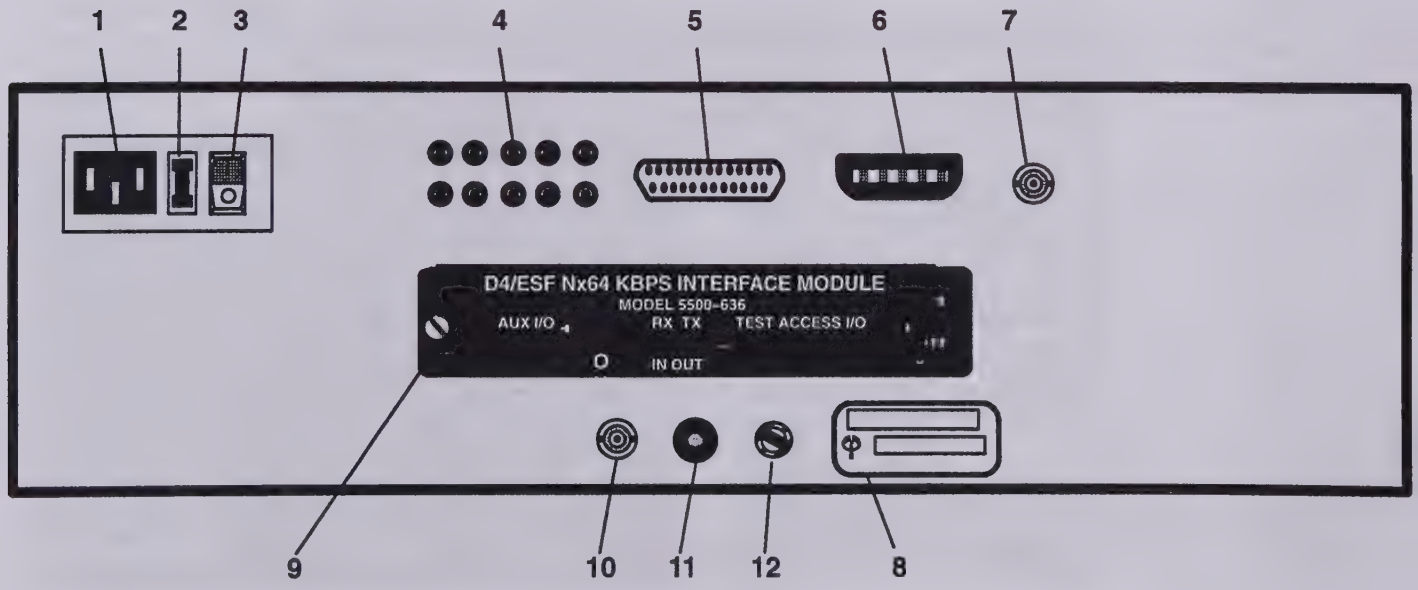


Figure 2–2. Model 5500A Rear Panel Controls and Indicators.

2.2 MENUS

The 5500A uses 14 standard menus which are arranged in a matrix as illustrated on the 5500A front panel. This section of the manual defines all the standard menus for the RS–232 module and the differences in those menus when the 5500A–636 ESF T1 module is inserted into the 5500A.

2.3 MENU SELECTION

The user can move between menus in one of two ways; menu matrix or direct access.

2.3.1 Menu Matrix Method

Menus are accessed by utilizing the menu matrix selection key. Movement is made by pressing the up, down, left, or right menu keys. The menu matrix guide (Figure 2–3) adjacent to the menu matrix selection key, is used for a guide only. Menus cannot be selected by pressing the guide overlay.

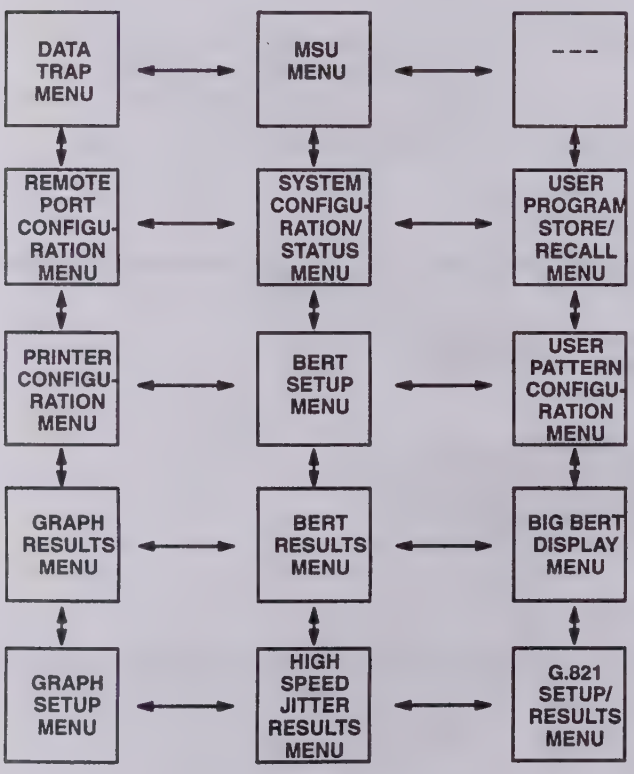


Figure 2–3. Menu Matrix.

2.3.2 Direct Menu Access Method

Menus can be directly accessed by pressing the HELP–1/RECALL–2 softkey once. The HELP Menu (Figure 2–4) is then presented. Press a valid menu selection (0–F on the HEX keypad) to obtain direct screen access. Then press the GO TO softkey in the menu. The active menu blinks in the direct menu access menu. Refer to paragraph 2.4.

2.4 MENU DESCRIPTIONS

2.4.1 HELP Menu

The HELP Menu, Figure 2–4, displays all the menus. This menu is basically the same for all interface options. To use this menu, proceed as follows:

1. Press the HELP–1/RECALL–2 key one time to display the HELP Menu.

2. The softkey for this menu is labeled GO TO on the menu and is the bottom softkey on the front panel (refer to Figure 2–1). Pressing this softkey displays the menu selected by the cursor. In Figure 2–4, the cursor is shown over menu #8, Graph Results. If the softkey were pressed in this example, the Help Menu would be replaced by the Graph Results Menu. Menus that are preceded with an identifier (*BERT Setup and *BERT Results/Parameters, #Printer Setup and

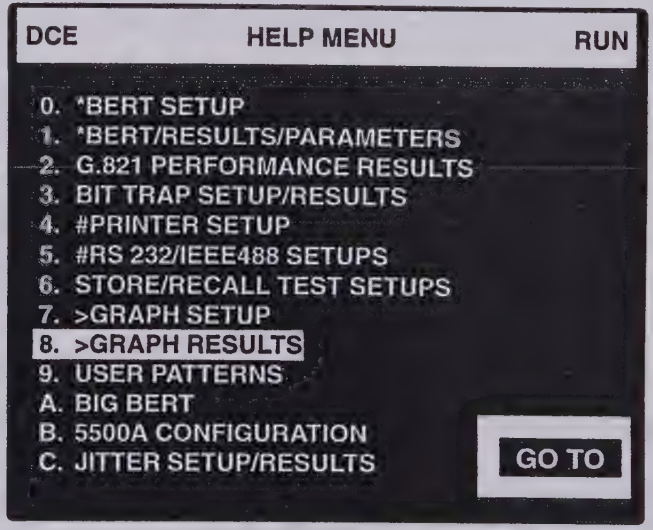


Figure 2–4. HELP Menu

3. The cursor can be moved on this menu by pressing a number or letter on the keypad which will move the cursor directly to the corresponding number on the list of menus.

2.4.2 5500A CONFIGURATION Menu

The 5500A CONFIGURATION Menu (Figure 2–5), is used to view 5500A system operation and provide a method to lock various controls.

The softkeys for this menu are the Master Lock and Options Menu select (paragraph 2.4.3). When the LOCK softkey is pressed, all the front panel controls listed on this menu are disabled. When the UNLOCK softkey is pressed, all of the previously locked function keys on this menu are unlocked. It is always a good idea to press the UNLOCK softkey prior to setting up the 5500A to run any test. Failure to notice that one of the front panel keys has been locked out can cause the user to spend many needless hours agonizing over how to get the 5500A to perform a particular function.

The following paragraphs explain the lines presented on the 5500A Configuration Menu (Figure 2–5).

1. This line reflects DCE, DTE, or the termination status of the module (LOOP, BRDG, TERM).

2. This area of the display is used to present the results to the 5500A power up self–test. The ROM, RAM, USER PROGRAM, and USER PATTERN are checked. The OPT line lists the various interface options and/or jitter options that are installed.

3. This area of the display allows the user to set the status of the front panel controls on the 5500A. By placing the cursor over the letter to the right of the control name, pressing the cursor select keys will scroll the letter from P to U to L. The L indicates the control is locked. Pressing the key will have no effect. The U indicates the key is unlocked. Pressing it will cause it to function in its normal manner. P indicates the key is protected and cannot be unlocked until the UNLOCKED key is pressed.

2.4.3 SYSTEMS OPTIONS Menu

When the OPTION softkey is pressed at the 5500A CONFIGURATION Menu, the SYSTEM OPTIONS SETUP Menu (Figure 2–6), is displayed. This menu is used to establish operating parameters for the 5500A as follows:

2.4.3.1 CRT REFRESH

The 5500A CRT is refreshed at a frequency that is a multiple of the line frequency. The user must set the line frequency using this line of the display. Use the **CURSOR** keys to place the cursor over the CRT REFRESH field and use the **SELECT** keys to select 50 Hz or 60 Hz.

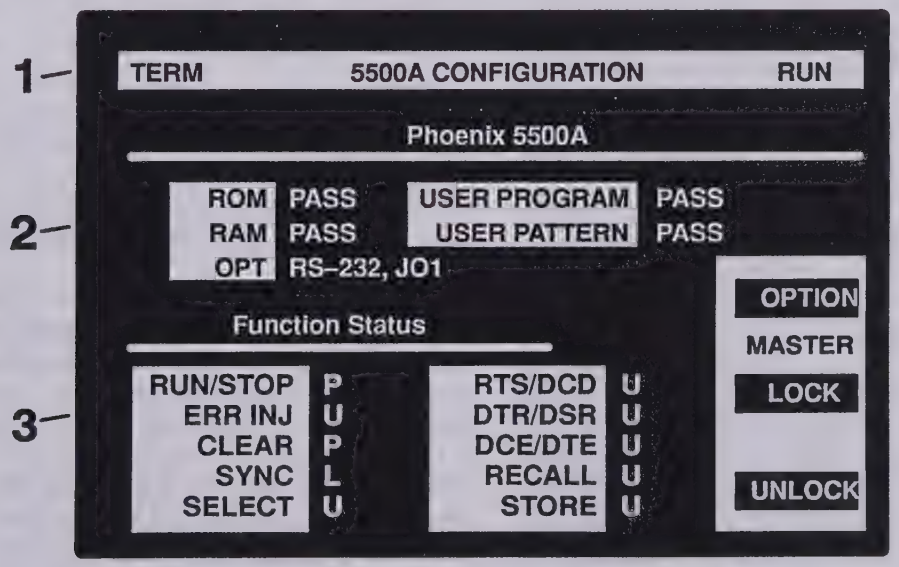


Figure 2–5. 5500A CONFIGURATION Menu.

2.4.3.2 SCREEN SAVER

The screen saver option turns off the CRT display approximately 10 minutes after the last key was pressed on the 5500A. Press any key on the 5500A to turn the display back on for another 10 minutes. This option is DISABLED or ENABLED by moving the cursor over the SCREEN SAVER field and using the the **SELECT** keys to select DISABLED or ENABLED.

2.4.3.3 GRAPH FORMAT

There are two ways the graph may be printed out on a printer. The LONG presentation is most frequently used and prints the entire graph data in a bar graph format. The SHORT presentation prints all the numeric data but does not print the bars on the graph. This option is most often used to conserve bits when the graph data is being sent to a remote site via a modem. Selection of LONG or SHORT is made with the **CURSOR** and **SELECT** keys in the same manner as the previous selections.

2.4.3.4 SCREEN ALIGN

This option is used to select CHAR SET or ALIGN #1 screens to be used to align the display on the face of the CRT during final pre–shipment testing of the 5500A. The alignment can be performed in the field, if required, by following the procedure below:

1. Select either of the alignment screens (CHAR SET or ALIGN #1). There is no difference in the alignment procedure between the alignment screens. Selection of the particular screen is a matter of user preference.
2. Press the **PAT** softkey. (The display will change to the selected screen alignment pattern.)
3. Use the **CURSOR** keys to move the display on the screen to the desired location.
4. Press a **SELECT** key to return to the SYSTEM OPTIONS SETUP Menu.

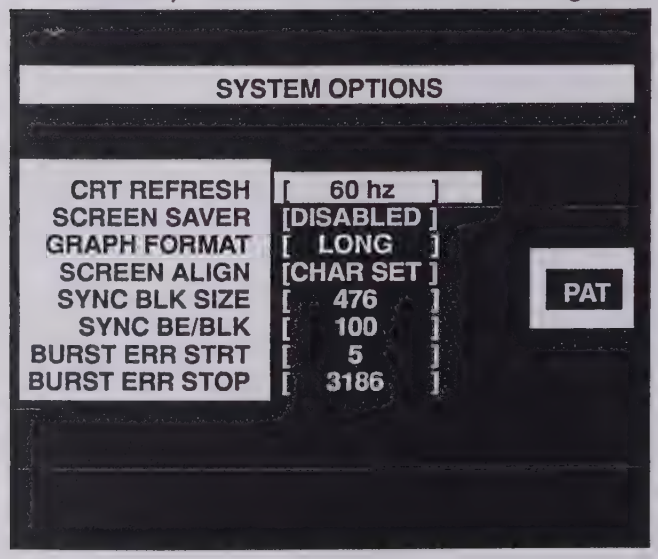

SYSTEM OPTIONS
CRT REFRESH [60 hz]
SCREEN SAVER [DISABLED]
GRAPH FORMAT [LONG]
SCREEN ALIGN [CHAR SET]
SYNC BLK SIZE [476]
SYNC BE/BLK [100]
BURST ERR STRT [5]
BURST ERR STOP [3186]
PAT

Figure 2–6. SYSTEMS OPTIONS Menu.

2.4.3.5 SYNC BLK SIZE SYNC BE/BLK

These two lines are used to establish the threshold for sync loss. The block size may be set to any value between 1 and 100,000 and the bit errors per block may be set to any value between 3 and 50,000. The factory setting of these values are a block size of 1000 with a bit errors per block of 100 or an error rate threshold of 1E–01.

To set a value to either line, place the cursor over the desired field and use the front panel HEX keypad to enter the desired value.

NOTE The values selected for block size and bit errors per block remain stored in memory and will not default to the factory setting on power up.

2.4.3.6 BURST ERR STRT BURST ERR STOP

The 5500A has incorporated a burst error detection circuit to aid the user in determining the distribution of errors. Burst errors (BURS on the ESF T1 BERT Results Menu) are considered a group of errors so closely grouped that for all intents and purposes, they are "one event".

These two lines of the System Options display are used to set the starting and ending error thresholds that define a "burst". The burst error start may be programmed from 1 to 15 consecutive errors while the burst error stop may be programmed from 1 to 50,000 consecutive error free bits.

This feature is particularly useful when a long term, unattended test is being run. Assume that the burst error start has been set to 1 consecutive bit errors and that 1000 consecutive error free bits has been selected as the burst error stop threshold. After a 24 hour period, the 5500A indicates that 74 bit errors took place, but only one burst

error took place. The user then knows that all the bit errors took place in one "burst" and except for that period of time, the circuit under test was error free.

2.4.4 BERT SETUP Menu

The BERT SETUP Menu, located at position 0 on the HELP Menu, is used to set up the majority of the test conditions. The menu is brought to the display by the following steps:

1. Perform the power up procedure (paragraph 3.1).
2. Press the HELP–1 key one time to bring the HELP Menu to the display.
3. Press the 0 key on the keypad.
4. Press the GO TO softkey.

The BERT SETUP Menu (Figure 2–7), should now be present on the screen. The synchronous and asynchronous mode setups are the same for the RS–232 and RS–449 modules.

2.4.4.1 RS–232 BERT SETUP Menu

The RS–232 BERT SETUP Menu is illustrated in Figure 2–7. The key line numbers correspond to the numbers below that explain each line of the menu. The softkey for this menu is the LOOP key which places the 5500A in the self–test loopback mode. Changes are made on this menu by moving the cursor over the desired parameter and then using the cursor SELECT keys to scroll the desired value under the cursor.

The lines on the BERT SETUP Menu are as follows:

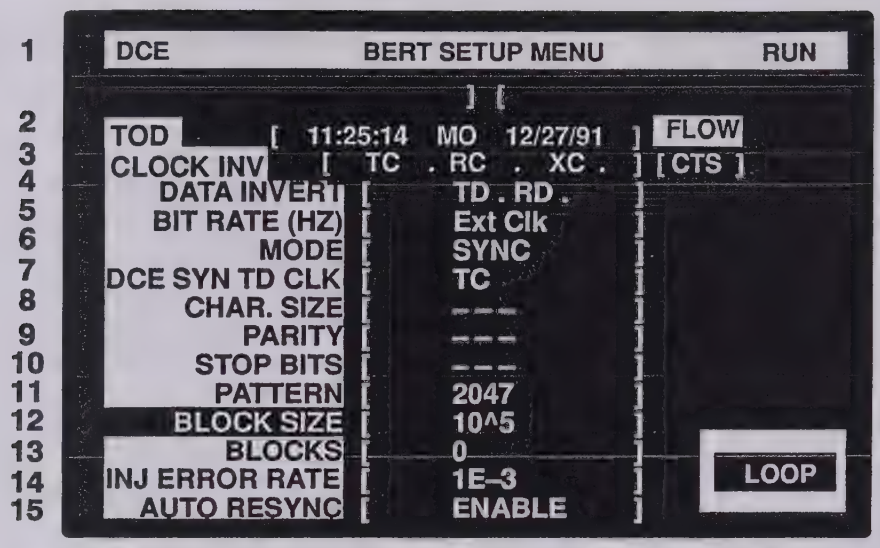
1. DTE/DCE – This section of the top line indicates what the 5500A is emulating, DTE or DCE.
2. TOD – This line contains the time of day and day/date/year. The correct time/date is set on this menu and once set, the information is retained in memory.
3. CLOCK INV – The user may elect to invert the polarity of the transmit (TC), receive (RC) or external (XC) clock signals. A dot (.) following the clock indicates the clock is NOT inverted. To invert the clock, place the cursor over the dot and press the CURSOR SELECT key. The dot will be replaced with an "I", indicating that clock has been inverted.
4. DATA INVERT – This line works in the same manner on the receive data (RD) and transmit data (TD) as the clock invert above.
5. BIT RATE – The internal bit rates which can be selected are listed in Figure 2–7. The O or S field choice to the left of the bit rate field refers to the optional specific frequency which the user may choose to enter. The synthesizer permits the user to select any data rate by entering the frequency through the use of the HEX keypad. By selecting the S field, the user may select any of the standard bit rates. The USER CLK choice refers to the rear panel clock input on the 5500A. The user may input a frequency synthesizer to the USER CLK BNC connector and select any frequency from 50 bps to 13 Mbps (dependent on the interface module) for operation.

   When configured as a DTE, transmit timing can be derived from RC when in the "Rec Clk" mode.

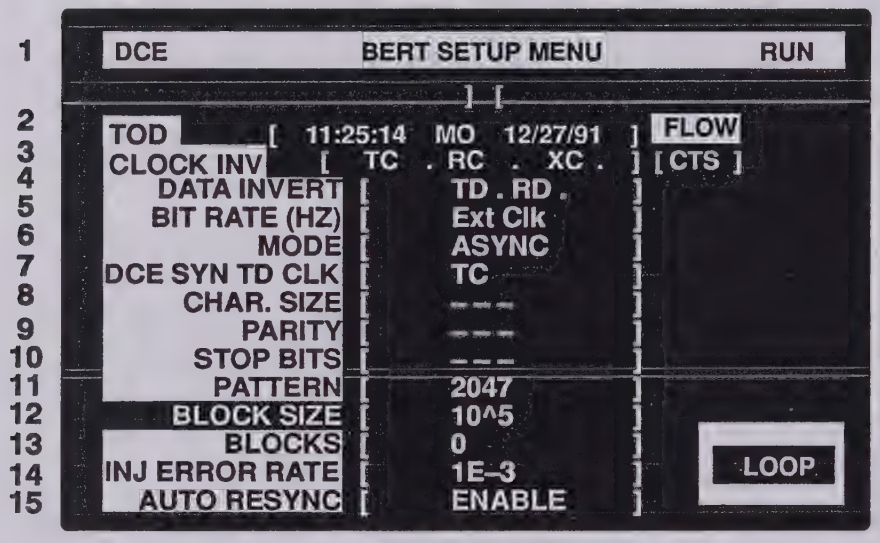
   Data is clocked out TD with the RC clock going out on XC.

   The HEX keypad is used to enter the bit rate and edit the bit rate field. The "0 – 9" keys are used to enter the numbers into the bit rate field. After the desired bit rate is entered, the "E" key is used to enter the bit rate selected. The "C" key serves as a CLEAR or DELETE key and will delete the last entry made. This key may be used in either the 'edit' or 'select' mode. The "D" key serves as the decimal point in those bit rates between 50.0 and 499999.9. For selections greater then 499999.9, the D key is not valid and the 5500A will respond with a 'BEEP' if the D key is used outside its range.
6. MODE – The 5500A is capable of synchronous or asynchronous operation. Generally speaking, most systems operating at 2400 baud and above are synchronous with the exception of certain compressed bit rate voice systems. The 5500A can operate at bit rates up to 72 Kbps asynchronously.

   In asynchronous operation, all transmitted data is characterized by the inclusion of a specific number of data bits, stop bits, and parity check. The user must select these items and they are described in steps 8, 9, and 10 that follow.
7. DCE SYN TD CLK – (DCE mode synchronous transmit data clock) When the user selects DCE simulation operation of the 5500A it is necessary to then select


DCE
BERT SETUP MENU
RUN
TOD [11:25:14 MO 12/27/91]
CLOCK INV [TC . RC . XC .]
DATA INVERT [TD . RD .]
BIT RATE (HZ) [Ext Clk]
MODE [SYNC]
DCE SYN TD CLK [TC]
CHAR. SIZE [- - -]
PARITY [- - -]
STOP BITS [- - -]
PATTERN [2047]
BLOCK SIZE [10^5]
BLOCKS [0]
INJ ERROR RATE [1E–3]
AUTO RESYNC [ENABLE]
FLOW
[CTS]
LOOP

SYNCHRONOUS MODE


DCE
BERT SETUP MENU
RUN
TOD [11:25:14 MO 12/27/91]
CLOCK INV [TC . RC . XC .]
DATA INVERT [TD . RD .]
BIT RATE (HZ) [Ext Clk]
MODE [ASYNC]
DCE SYN TD CLK [TC]
CHAR. SIZE [- - -]
PARITY [- - -]
STOP BITS [- - -]
PATTERN [2047]
BLOCK SIZE [10^5]
BLOCKS [0]
INJ ERROR RATE [1E–3]
AUTO RESYNC [ENABLE]
FLOW
[CTS]
LOOP

ASYNCHRONOUS MODE

BIT RATES THAT MAY BE SELECTED ON LINE 5

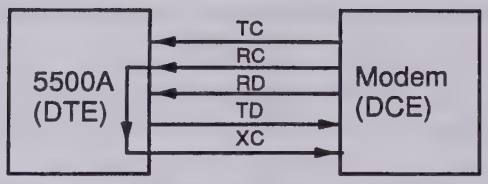
(Must be in standard (S) mode – optional mode (O) permits selection of any rate between 50 Hz and 13 MHz. Rates in **bold** may only be selected in SYNC mode).

BPS			KBPS				MBPS	
75	110	134.5	14.4	16	19.2	24	1.024	
150	200	300	28.8	32	48	56	1.544	
600	1200	1800	57.6	64	72	**76.8**	OTHER	
2400	3200	3600	**84**	**96**	**112**	**115.2**	Opt Clk	
4800	6400	7200	**128**	**144**	**153.6**	**168**	**Ext Clk**	
8000	9600		**192**	**224**	**230.4**	**256**	User Clk	
			288	**336**	**384**	**448**	**Rec Clk**	
			460.8	**512**	**576**	**672**		
			768					

PATTERNS AVAILABLE ON LINE 11

63, 511, 2047, REV 2047, (2^15)–1, (2^20)–1, QRW, LOOP–UP, LOOP–DN, MARK, SPACE, ALT, FOX, FOX2, SYSY 511, X25 511, (2^9)–1 A, NET55, 1:7, 3:24, USR1, USR2, USR3, USR4.

Figure 2–7. RS–232 BERT SETUP Menu.



whether the test set (simulating a MODEM) will supply clock (TC–Pin 15) to, or derive clock (XC–Pin 24) from the system under test in synchronous operation. If the user selects TC then the 5500A transmitter's clock source is its own internal clock. If XC is chosen then the 5500A transmitter derives its timing from the system under test. Note that this selection is only meaningful in synchronous DCE mode simulation and is primarily used only when operating at speeds greater than 1 MHz.

8. CHAR SIZE – The number of data bits which make up a character in asynchronous data transmission is selectable from either the BERT SETUP or BERT RESULTS menus. Asynchronous character sizes of 5, 6, 7, or 8 bits length may be chosen. If CONTINUOUS is chosen, then the 5500A sends out a continuous stream of data bits without start and stop bits. When operating in a synchronous mode there are no start and stop bits and so the bit stream is continuous or infinite and three dashes are displayed in the menu field.

9. PARITY – Parity bits in the data stream provide a means of error detection. In async data streams the user may select EVEN or ODD parity or may choose NO parity at all. Choosing EVEN parity means that the number of 1's in a data block must add up to an even number. Likewise ODD parity means the number of 1's in the block of data sums up to an odd number. If, in EVEN parity, a block is received with three 1's in it, then the detector knows there has been at least one error. The choice of parity or no parity depends entirely on the system under test. The parity bits are not used in synchronous data streams, therefore three dashes appear in parity field when the synchronous mode has been selected.

10. STOP BITS – Asynchronous, Byte oriented data transmissions employ start and stop bits to identify one byte from the next. A typical data transmission may be composed of a start bit, seven data bits, a parity bit, and a stop bit. The choice of STOP BITS is either 1 or 2 and depends upon the system under test. This parameter has no meaning in synchronous transmission, and therefore the field contains three dashes.

11. PATTERN – The choice of pattern depends upon the test which the user desires to make. The 5500A uses industry standard pseudorandom sequences of various lengths for Bit Error Rate testing (Figure 2–7), plus a number of other patterns for specific uses, as well as four USER programmable patterns. Three patterns can be up to 135 HEX characters long. USER PATTERN #4 may be up to 2200 characters long.

    A **FOX** pattern is available for testing low speed applications and is as follows:

    THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK

    A **FOX–2** pattern is available for testing low speed applications and is as follows:

    THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK 0123456789 CR, LF

    When used in the async mode, the character size selection also sets the coding format as follows:

Character Size	Code Format
5	BAUDOT
6	EBCDIC
7	ASCII
8	BCDIC

    In the synchronous mode the FOX–2 pattern is coded as 8–bit ASCII.

    A **NET 55** stress pattern is also available which is as follows:

    01 01 03 01 01 01
    00 01 01 01 01 01
    01 03 01 01 01 01
    07 01 01 01 01 55
    55 55 55 AA AA AA
    AA 01 01 01 01 01
    01 FF FF FF FF FF
    FF 80 01 80 01 80
    01 80 01 80 01 80 01

    The **1:7** pattern is useful for testing minimum 1's density requirements. It can be used unframed or D4/ESF framed. It is as follows:

    0100 0000 0100 0000 0100 0000

    The **3:24** pattern may be run unframed or D4/ESF framed. It is useful for stressing minimum 1's density and maximum 0's allowed on AMI lines.

    0010 0010 0000 0000 0010 0000

    The other pattern selections are as follows:

63, 511, 2047, REV2047, LOOP–UP, LOOP–DN, MARK, SPACE, SYSY 511, X25 511, (2^9)–1 A, and the following:

The **ALT** (1:1) pattern, when framed, the 1's in this pattern are offset from the beginning of the sequence and the pattern is transmitted repetitively as FR 010101.... This insures bit 2 does not cause a yellow alarm.

The relative frequency of this pattern is >72kHz, where if an analog tone was represented by the digital pattern, a frequency where a dip in voltage level would occur if the line were to be frequency swept with an analog signal. Note that an analog tone used for such tests would not pass through a repeater requiring that each section of the span line be tested on a individual basis.

The 1:1 represents a 50% 1's density and has no useful purpose for B8ZS or HDB3 line coding.

63 – 63–bit Pseudorandom Pattern for low speed data applications.

511 – 511–bit Pseudorandom Pattern for low speed data applications.

2047 – 2047–bit Pseudorandom Pattern for low speed data applications.

REV2047 (2047–bit Pseudorandom Pattern) – is the same as the 2047 pattern except it is shifted out in the serial bit stream in reverse order.

LOOP–UP is the CSU loop up code transmitted as one 1 and 4 zeros (10000).

LOOP–DN is the CSU loop down code transmitted as one 1 and 2 zeros (100).

SYSY 511 – same as 511 pattern with two sync characters between (16, 16).

X25 511 – 511 pattern with check sum sequence imbedded.

(2^9)–1A – 511 pattern with tap points taken at bits 3 and 8.

2^15–1 (32,757–bit Pseudorandom Pattern) – is a pseudorandom pattern which generates a maximum of 14 sequential zeros and 15 sequential ones. The pattern provides a maximum number of zeros allowed for framed, non–B8ZS testing. The pattern does not meet the ones density requirement.

2^20–1 (1,048,575–bit PRBS) – is a pseudorandom pattern which generates a maximum of 19 sequential zeros and 20 sequential ones. The pattern exceeds excess zeros and does not meet the ones density requirement for T1 applications. Is useful for stress testing circuits provisioned for B8ZS.

QRW – simulates live data for T1 applications. T1 QRSS allows 14 sequential zeros and 20 sequential ones.

MARK – F1111; contains maximum amount of energy. Useful for stressing power dissipation capabilities of line repeaters.

SPACE – All zeros; effective B8ZS stress test.

12. BLOCK SIZE – The number of bits which make up a block can be selected as follows:

10^2	100 bits/block
10^3	1,000 bits/block
10^4	10,000 bits/block
10^5	100,000 bits/block
10^6	1,000,000 bits/block
10^7	10,000,000 bits/block
10^8	100,000,000 bits/block
10^9	1,000,000,000 bits/block

The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks in the test equals a specific number of bits. The choice of block size may be dictated by any number of factors, however, normally the higher the bit rate, the larger the block size.

13. This line may be set to BLOCKS or TEST TIME by placing the cursor over BLOCKS or TEST TIME and using the **SELECT** keys to toggle between the two choices.

When BLOCKS has been selected, the number of blocks in the test may be selected as any number from 1 to 9999. If a "0" is placed in this window, then the 5500A will run a test continuously until the **STOP** key is pressed. If a number is entered in the BLOCKS field, the test will stop when the number of blocks tested is equal to the number entered in the BLOCKS field.

The user selects BLOCKS by moving the half intensity marker to the field to the right of BLOCKS and setting the desired number using the HEX front panel keypad.

When TEST TIME has been selected in this field, the length of time that the test is to be run is entered in the field to the right of TEST TIME through the use of the front panel keypad. The 5500A will stop the test after the selected time increment has elapsed. Entering 00:00:00 will result in a continuous running test.

NOTE The 5500A sends an automatic "Service Request" on the IEEE488 bus at test end.

14. INJ ERROR RATE – The 5500A enables the user to inject single or multiple bit errors at rates from 5E–2 to 1E–9 errors/bit. The user must select the rate to be injected at the ERROR INJECT RATE field in the BERT SETUP Menu. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the desired rate using either the SELECT keys or the HEX keypad. The choices are 0 to 9. A "0" (zero) will disable the error inject. Then the user must use the CURSOR key to move the block to the right and change the exponent from –2 to –9 as desired. Once set, the rate is retained in non–volatile memory. To inject a single logic error, enable then quickly disable the **INJ** softkey while at the BERT RESULTS Menu. Error injection is most often used for identification and testing the integrity of a circuit.

15. AUTO RESYNC – The auto resync function in the 5500A has three states; enable, disable, and timed. When the auto resync feature is disabled, the 5500A will continue to count bit errors once synchronization has been lost, regardless of the number of bit errors per unit time. When the auto resync is enabled, the 5500A obtains synchronization and then continually monitors the bit error count and, when the bit error rate exceeds a predetermined threshold, the 5500A will declare it has lost synchronization and will not recover synchronization until a preset number of error free bits are achieved, usually set at 56 bits. During this time the 5500A is out of synchronization, error parameter collection is suspended, with only the time the unit is out of synchronization being accumulated.

    In the timed resync mode, a number of 10 millisecond intervals (0–999, representing 0 to 9.99 seconds) is selected by the user as the time span of an internal timer. During the time cycle, if at least one bit error occurs during each 10 millisecond interval, the 5500A will count these errors until the timer runs out. When the timer runs out, the 5500A will check the bit error sync threshold to determine if sync should be broken. If the 5500A breaks sync, it will enter the auto resync disable mode and restart the internal timer. During the timer period, two events are taking place; 1) the 5500A is continuing to accumulate bit errors and, 2) the 5500A is monitoring the data to determine if errors have ceased. If only one 10 millisecond interval is error free, the timer is reset. If errors have ceased, the 5500A continues and the timer is reset, awaiting the next bit error occurrence.

16. FLOW – The FLOW field may be set to OFF or CTS. In the CTS mode, when the 5500A is configured as a DTE and CTS is driven true, the 5500A's transmitter will stop transmitting data to the DCE direction. When CTS is driven false, the 5500A will again enable the transmitter. If CTS is off, it has no effect on the transmitter.

2.4.4.2 T1 ESF BERT SETUP Menu

The T1 ESF BERT SETUP Menu is illustrated in Figure 2–8. The key line numbers correspond to the numbers below that explain each line of the menu. There are three softkeys for this menu. The bottom softkey is the **LOOP** key which places the 5500A in the self–test loopback mode. The top two softkeys are used to select the appropriate termination mode; Bridge, Terminate, or Monitor using the following guidelines:

NOTE Activate the **MON** key (top) to the "highlighted" state for "MONITOR" mode. Deactivate the **MON** key to return to the highlighted BRDG or TERM mode. The middle softkey is an alternate function **TERM/BRDG** key. Activate this softkey to change from the displayed mode (i.e., TERM) to the alternate mode (i.e., BRDG).

BRDG mode (Bridge) high impedance termination option; SAFEST for the curious when wishing to avoid interference with the monitored circuit.

TERM mode terminates the RX pair with 100 ohms and is used only when the circuit being tested "terminates" at the Model 636 test interface. It is normally used in out–of–service testing when the test set is substituted for the normal network terminating device.

MON (Monitor) mode is specifically for DSX panel test access via a standard DSX "Monitor" jack which provides two 430 ohm resistors in series with tip and ring. In this mode the test set will terminate the RX pair with 100 ohms, resulting in 20dB attenuation of the resistor isolated monitor signal. The resistors minimize circuit interference which might otherwise result from the test set load impedance, test probe contact bounce transients, or an improper test connection to a transmitter instead of a

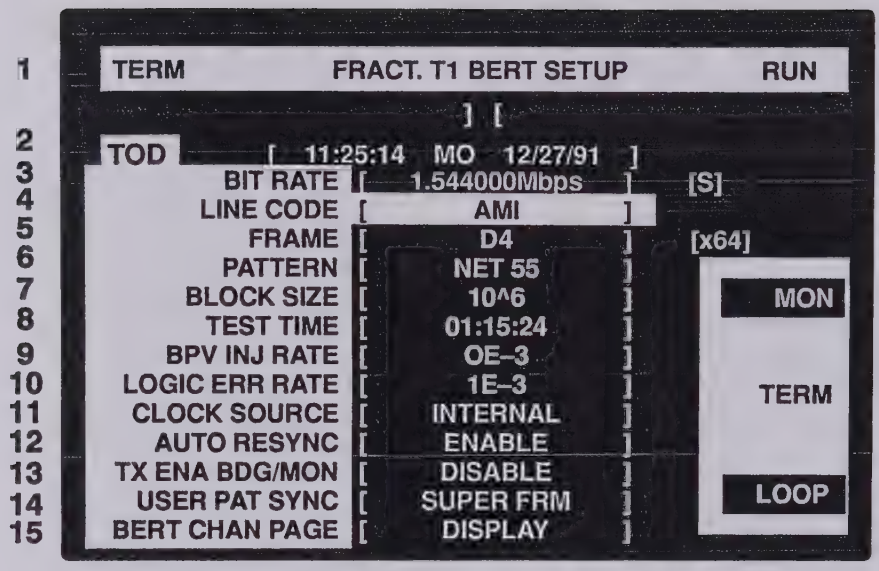


Figure 2–8. FRACT T1 BERT SETUP Menu.

receiver. The Monitor mode invokes a 20dB amplifier (voltage gain of 10) to compensate for the 20dB attenuation of the 430 ohm resistors. Monitor jack remote test access wire lengths in excess of 2000 feet may be accommodated by using standard, Z0=100 ohm wiring, with the 636 module in the Monitor mode.

Changes are made on this menu by moving the cursor over the desired parameter and then using the cursor SELECT keys to scroll the desired value under the cursor.

The following is a description of the lines on the FRACTIONAL T1 BERT SETUP Menu:

1. This line gives the status of the termination mode selected (TERM, BRDG, MON) with the softkeys as described above.

2. TOD – This line contains the time of day and day/date/year. The correct time/date is set on this menu and once set, the information is retained in memory.

3. BIT RATE (Hz) – This line shows the bit rate for the interface module (in this case T1). There are two fields associated with this line. The O or S field to the left of the bit rate line permits the user to select S for the standard bit rate for the module (in this case, 1544000). By selecting O, the operator may choose any bit rate desired through the use of the front panel keypad. Only the frequency within a specific range will work with this module (±300Hz).

4. LINE CODE – This line is used to select the desired line code, AMI (alternate mark inversion) or B8ZS (bit eight zero substitution).

5. FRAME – This line is used to select the framing format desired. Choices are SLC®96, ESF, D4, or DISABLE. The DISABLE selection would be made if it was desired to test unframed data at the T1 data rate.

6. PATTERN – The choice of pattern depends upon the test which the user desires to make. The 5500A uses industry standard pseudorandom sequences of various lengths for Bit Error Rate testing (Figure 2–7) plus a number of other patterns for specific uses as well as a USER programmable pattern up to 2200 HEX characters long.

   The NET55 pattern is for those users that have been using the 2^{15}–1 pattern as an alternative to the QRW pattern to stress test T1 network facilities. Unfortunately, the 2^{15}–1 pattern violates the 1's density specification in publication 62411 thus giving span vendors the option of ignoring the test results.

   The NET55 stress pattern meets all the specifications in publication 62411. It has also been proven in field trials as being able to cause marginal spans to fail more consistently than the 2^{15}–1 or the QRW patterns. Phoenix suggests that the NET55 pattern be run with the frame disabled in the T1 setup.

7. BLOCK SIZE – The number of bits which make up a block can be selected as follows:

10^2	100 bits/block
10^3	1,000 bits/block

10^4	10,000 bits/block
10^5	100,000 bits/block
10^6	1,000,000 bits/block
10^7	10,000,000 bits/block
10^8	100,000,000 bits/block
10^9	1,000,000,000 bits/block

The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks in the test equals a specific number of bits. The choice of block size may be dictated by any number of factors, however, normally the higher the bit rate, the larger the block size.

8. This line may be set to BLOCKS or TEST TIME by placing the cursor over BLOCKS or TEST TIME and using the **SELECT** keys to toggle between the two choices.

   When BLOCKS has been selected, the number of blocks in the test may be selected as any number from 1 to 9999. If a "0" is placed in this window, then the 5500A will run a test continuously until the **STOP** key is pressed. If a number is entered in the BLOCKS field, the test will stop when the number of blocks tested is equal to the number entered in the BLOCKS field.

   The user selects the BLOCKS by moving the half intensity marker to the field to the right of BLOCKS and setting in the desired number using the HEX keypad numbers.

   When TEST TIME has been selected in this field, the length of time that the test is to be run is entered in the field to the right of TEST TIME. In the example shown in Figure 2–8, a test length of 1 hour 15 minutes and 24 seconds has been entered through the use of the HEX keypad numbers. The 5500A will stop the test after the selected time increment has elapsed. Entering 00:00:00 will result in a continuous running test.

NOTE The 5500A sends an automatic "Service Request" on the IEEE488 bus at test end.

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9. INJECT RATE – This line is a dual function line. The first choice the user has to make is the type of errors to be injected. This is accomplished by moving the cursor over the black area (where it says BPV INJ RATE in Figure 2–8) on the menu. The user then may select from the following:

   BPV INJ RATE, F BIT INJ RATE, CRC INJ RATE, or D INJ(CRCrate) in ESF mode.

   BPV INJ RATE, F BIT INJ RATE, or S BIT INJ RATE in D4 mode.

   BPV INJ RATE or F BIT INJ RATE in SLC96 mode.

NOTE The available inject modes are automatically restricted to those appropriate for the selected combination of FRAME and CLOCK SOURCE modes (refer to Table 2–3). Additional information on the inject modes can be found in the instruction manual for the specific module you have installed in the 5500A. (Refer to the Option section of this manual.)

Table 2–3. Error Injection Modes.

FRAME	CLK	BPV INJ	FBIT INJ	SBIT INJ	DATA INJ	CRC INJ
D4	INT	X	X	X		
D4	EXT	X	X	X		
D4	RX	X	X	X		
D4	THRU	X	X	X	X	
D4	DROP/INS	X	X	X	X	
D4	DROP/INS–J (JO2)	X	X	X	X	
D4	DROP/INS+J (JO2)	X	X	X	X	
D4	JIT(02)	X	X	X		
D4	THRU–J(JO2)	X	X	X	X	
D4	THRU+J(JO2)	X	X	X	X	
SLC®96	INT	X	X			
SLC®96	EXT	X	X			
SLC®96	RX	X	X			
SLC®96	THRU	X	X		X	
SLC®96	DROP/INS	X	X			
SLC®96	DROP/INS–J (JO2)	X	X			
SLC®96	DROP/INS+J (JO2)	X	X			
SLC®96	JIT(JO2)	X	X			
SLC®96	THRU–J(JO2)	X	X		X	
SLC®96	THRU+J(JO2)	X	X		X	
ESF	INT	X	X		X	X
ESF	EXT	X	X		X	X
ESF	RX	X	X		X	X
ESF	THRU	X	X		X	X
ESF	DROP/INS	X	X		X	X
ESF	DROP/INS–J (JO2)	X	X		X	X
ESF	DROP/INS+J (JO2)	X	X		X	X
ESF	JIT(JO2)	X	X		X	X
ESF	THRU–J(JO2)	X	X		X	X
ESF	THRU+J(JO2)	X	X		X	X
ESF	USER	X	X		X	X
UNFRAMED						
DISABLE	INT	X				
DISABLE	EXT	X				
DISABLE	RX	X				
DISABLE	THRU	X			X	
DISABLE	JIT(JO2)	X				
DISABLE	THRU–J(JO2)	X			X	
DISABLE	THRU+J(JO2)	X			X	

The second choice the user must make is selection of the inject error rate. The user programs the error rate by scrolling the half intensity block over the (——) INJ RATE field. The user must select the desired rate using either the SELECT keys or the HEX keypad. The choices are 1 to 9. Then the user must use the CURSOR key to move the block to the right and change the exponent from –3 to –7 as desired.

10. LOGIC ERR RATE – The 5500A permits the user to inject single or multiple bit errors at rates from 9x10–3 to 1x10–9 errors/bit. The user must select the rate to be injected at the ERROR INJECT RATE field in the BERT SETUP Menu. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the desired rate using either the SELECT keys or the HEX keypad. The choices are 0 to 9. A 0 (zero) will disable the error inject. Then the user must use the CURSOR key to move the block to the right and change the exponent from –3 to –9 as desired. Once set, the rate is retained in non–volatile memory. To inject a single logic error, enable then quickly disable the **INJ** softkey while at the BERT RESULTS Menu. Error injection is most often used for identification and testing the integrity of a circuit.

11. CLOCK SOURCE – There are eight (five without the J02 jitter option) possible selections for the source of the transmit clock timing for the "TX OUTPUT" of the 5500A–636 Module. These selections are; Rx, THRU, EXTERNAL, INTERNAL, USER, **JIT, THRU–J**, and **THRU+J**. The clock sources listed in bold are only available with the J02 jitter option. Table 2–4 presents detailed information on each clock source.

Table 2–4. Clock Source Selections for ESF T1.

CLOCK SOURCE	DESCRIPTION
INT CLK	Internal Oscillator (main chassis/not in module). Select INT CLK for any standalone equipment testing and anytime loop timing is not appropriate (someone in the network must originate the clock; everyone cannot slave to recivered clock).
RX CLK	"RX INPUT" recovered clock. Select RX CLK anytime the "TX OUTPUT" is required to be "loop timed" to the "RX INPUT" clock.
EXT CLK	TTL input via pins 15 (EXT CLK) and 36 (RETURN) of the 40–pin "TEST ACCESS I/O" connector. Connect any TTL external clock source @ 1544000+/–300 Hz for frequency tolerance testing of receivers, repeaters, etc. Connect any TTL precision clock, or network stratum 1 clock, etc., for use as: A) "TX OUTPUT" timing clock, and/or B) CSLP reference clock.
JIT CLK	The JO2 Option modulates the internal clock source as specified via the Jitter Option Menu. The amplitude and frequency of phase modulation (and modulation wave shape – sine, triangle, or external modulation source) may be controlled to evaluate the jitter tolerance of network components.
THRU	"RX INPUT" bit stream is retransmitted at "TX OUTPUT" with all data bits, frame bits, data link bits, bipolar violations, etc., unaltered. This mode may be used to provide an in–line repeater function (ALBO phase compensation, clock recovery, and retransmission of a nominal 6V peak–to–peak signal with 10%–30% trailing edge overshoot per Pub 62411). This mode also provides for injection of data errors, frame errors, etc. in live traffic for evaluation of error tolerance of command/response protocols, error checking algorithms, packet switching protocols, etc. (when the standard BERT pseudorandom test patterns are inappropriate).
THRU–J	Same as "THRU" above except the phase jitter (up to 10 unit intervals peak–to–peak) of the recovered "RX INPUT" clock is attenuated by approx. 40dB at 120 Hz (and above) to a level of less than .1 unit intervals peak–to–peak. This de–jittered clock is then used as the "TX OUTPUT" clock source. This mode may be used to sectionalize jitter tolerance problems, especially when the standard BERT pseudorandom test patterns are inappropriate and/or when extended out–of–service testing and trouble-shooting is not permitted.

Table 2–4. Clock Source Selections for ESF T1 (Cont.).

CLOCK SOURCE	DESCRIPTION
THRU+J	Same as "THRU" and "THRU–J" above except the "jitter attenuated", recovered "RX INPUT" clock is phase modulated as specified via the JO2 Jitter Option Menu, and then used as the "TX OUTPUT" clock source. This mode may be useful in characterizing the jitter tolerance margins (or shortcomings) of network components in "live traffic" situations.
USER	TTL LEVEL INPUT TO BNC ON BACK OF 5500A Connect any TTL external clock source @ 1544000 ± 300Hz for frequency tolerance testing of receivers, repeaters, etc. Connect any TTL precision clock or network stratum 1 clock, etc. for use as: a) "TX Ouput" timing clock and/or b) Clock slip (CSLP) reference clock
DROP/INSERT	Same as THRU mode except the test pattern is inserted in the active channels.
DROP/INSERT–	Same as THRU– mode except the test pattern is inserted in the active channels.
DROP/INSERT+	Same as THRU+ mode except the test pattern is inserted in the active channels.

12. AUTO RESYNC – The auto resync function in the 5500A has three states; enable, disable, and timed. When the auto resync feature is disabled, the 5500A will continue to count bit errors once synchronization has been obtained, regardless of the number of bit errors per unit time.

    When the auto resync is enabled, the 5500A obtains synchronization and then continually monitors the bit error count. When the bit error rate exceeds a predetermined threshold, the 5500A will declare it has lost synchronization and will not recover synchronization until a preset number of bits matches the pattern (usually set at 56 bits). During this time the 5500A is out of synchronization and error parameter collection is suspended, with only the time the unit is out of synchronization being accumulated.

    In the timed resync mode, a number of 10 millisecond intervals (0–999, representing 0 to 9.99 seconds) is selected by the user as the time span of an internal timer. During the time cycle, if at least one bit error occurs during each 10 millisecond interval, the 5500A will count these errors until the timer runs out. When the timer runs out, the 5500A will check the bit error sync threshold to determine if sync should be broken. If the 5500A breaks sync, it will enter the auto resync disable mode and restart the internal timer. During the timer period, two events are taking place; 1) the 5500A is continuing to accumulate bit errors, and 2) the 5500A is monitoring the data to determine if errors have ceased. If only one 10 millisecond interval is error free, the timer is reset. If errors have ceased, the 5500A continues and the timer is reset, awaiting the next bit error occurrence.

13. TX ENA BDG/MON –The TX OUTPUT jack is connected, tip and ring, to the secondary winding of the 636 transmitter output transformer via series relay contacts. The relay contacts are normally closed only in the "TERM" mode and open in the "BRDG" and "MON" modes (and open anytime "LOOP" is enabled). The "TX ENA BRDG/MON" ENABLE/DISABLE option allows the TX relay to be enabled or disabled in the Bridge and Monitor modes. The sleeve is connected to the test set "ground" circuit for shield termination.

14. USER PA SYNC – The user pattern sync mode may be off, frame, or superframe. These user pattern sync modes are provided for those test applications where you must be able to control bit patterns in specific channel time slots of the T1 signal.

    The frame mode will align a 24 byte user data pattern with T1 frame sync so that byte one of the user pattern is transmitted in the first time slot of the framed T1 signal, and byte two is the second slot and so on.

    The superframe D4 and SLC®96 mode will align a 288 byte pattern. For ESF, the 5500A will align a 576 byte pattern. The first 24 bytes go out in frame one of a superframe. The second 24 bytes go out in frame two, and so on. User patterns 1 thru 3 are limited to 135

bytes, so you must test with User Pattern 4 to test with superframe patterns. In this mode and the frame mode, the 4th, 5th, and 6th bytes of the user pattern are used for BERT sync and must be unique.

In some applications short patterns are used, such as special non–standard loop–up and loop–down codes for CSUs, repeaters, or other network equipment. To send these short patterns, set the user pattern sync to "OFF". The pattern will be sent repeatedly without frame alignment. In this mode the first three bytes of the user pattern are used for receive–user–pattern–sync and must be unique. (Refer to section 2.4.11 for additional information on patterns.)

15. BERT CHAN PAGE – To select the desired channels for fractional testing, place the cursor over the BERT CHAN PAGE field and press either of the SELECT keys. The menu shown in Figure 2–9 will appear on the screen.

    The "X" beside the channel indicates the channel is selected. If the channel is not selected, a dash ("–") appears beside the channel. Individual channels may be selected or deselected by moving the cursor to the desired channel and pressing either of the SELECT keys. To change the status of all the channels, press the ALL softkey. When the ALL softkey is pressed, the ALL softkey will change to read CLEAR and the SELECT softkey will change to read SET. Press the CLEAR softkey to deselect all the channels or the SET softkey to select all the channels.

    When you have completed your selections, you may store them and put them into effect by pressing the SELECT softkey. Pressing the CANCEL softkey will abort the edit session without putting the changes into effect. Pressing any MENU SELECT key will return you to the FRACT T1 BERT SETUP Menu.

    The effect of your selections will vary depending upon the clock mode you have selected. When the THRU mode is selected, all received data is sent back out to the network regardless of the selections. Only the receive data on the selected channels will be included in the test results.

    When the clock is set to EXTERNAL, INTERNAL, JITTER, or RECEIVE, the received data on all selected channels will be dropped and the selected test pattern transmitted to the network. Any channel not selected will be idled, with all ones being transmitted.

    In any drop/insert mode, the received data on selected channels will be dropped and the selected test pattern will be sent to the network. On deselected channels, the unit will pass received data directly back out to the network.

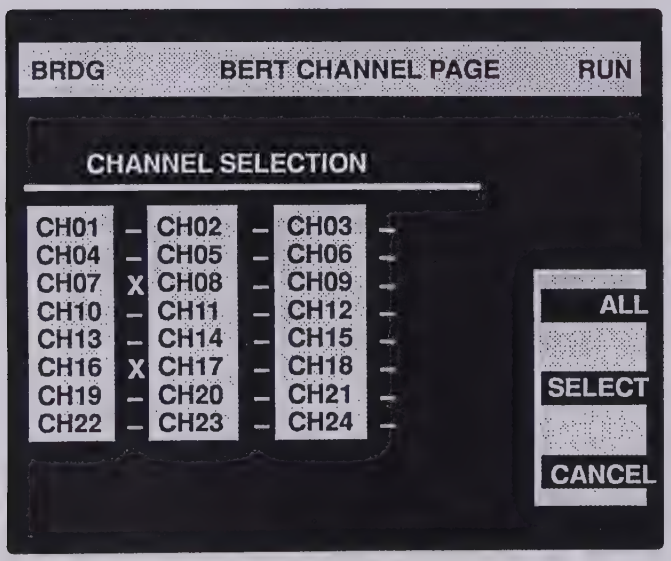


Figure 2–9. 5500A BERT CHANNEL PAGE Menu.

NOTE When jitter is injected or removed, all channels are affected regardless of the selections.

2.4.5 BERT Results/Parameters Menu

The primary purpose of the BERT RESULTS/PARAM menu is to view the results of a test, either as the test is running and/or when the test is completed. The 5500A monitors and keeps track of up to 45 parameters simultaneously depending upon the interface module installed.

To view the BERT Results/Parameters menu, follow these steps:

1. Perform the initial power up procedure in paragraph 3.1.
2. Bring the HELP Menu to the screen by pressing HELP one time.
3. Press the 1 key on the keypad.
4. Press the GO TO softkey.
5. The BERT Results/Parameters Menu should now be on the display.

2.4.5.1 RS–232 BERT Results/Parameters Menu

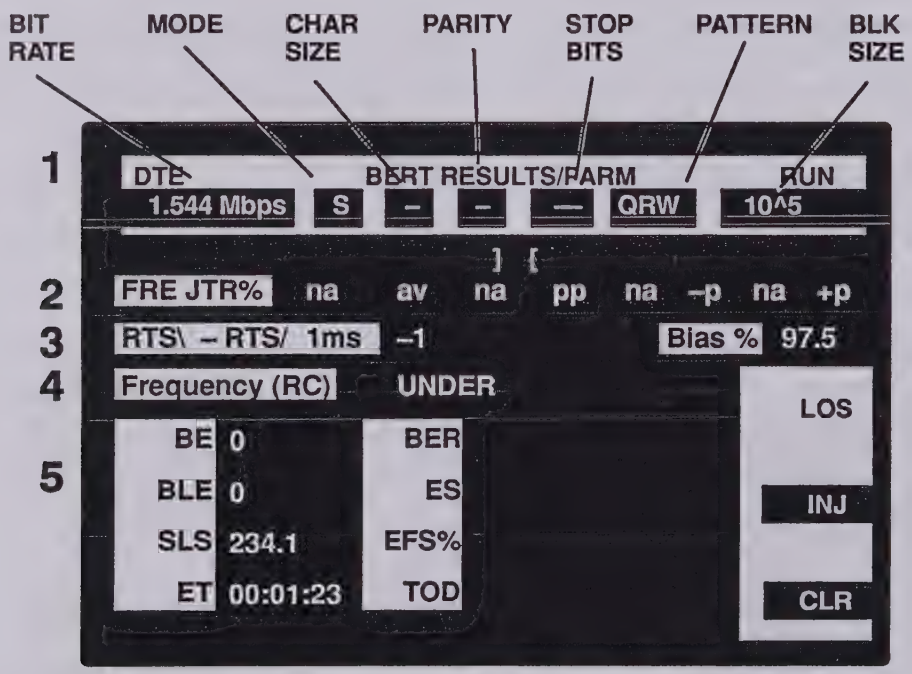
There are three softkeys for this menu (Figure 2–10). Their functions are as follows:

The top softkey is a reflection of the SYNC and SYNC REC LEDs on the front panel. When the 5500A is in the RUN mode, the top softkey will display BRK until sync is acquired. When sync has been acquired, the SYNC LED will turn on and the softkey will display SYNC. At this point in time, the softkey may be pressed to force a sync break if desired. If the 5500A looses sync, the SYNC LED will turn off and the softkey will display LOS (loss of sync). When the 5500A recovers sync, the SYNC REC LED and the SYNC LED will be turned on and the softkey will display REC. Pressing the softkey will reset the SYNC REC LED (turning it off) and change the softkey display to SYNC.

The second softkey (INJ) is used to turn the error injection on (INJ highlighted) or off (INJ as shown in Figure 2–10). To inject a single logic error, enable then quickly disable the INJ softkey while at the BERT RESULTS Menu.

The third softkey (CLR) is used to clear all the parameter counters and reset all the displays to zero. Pressing the CLR softkey will result in the display changing to 'OK?'. This is to prevent accidentally erasing test data. To clear the parameters the user must press the softkey again before the "OK?" is replaced with CLR (about 2 seconds).

1. The top line of this display identifies the menu, shows if DTE or DCE has been selected, and if the 5500A is in the RUN mode. The second line is a condensed version of the BERT SETUP Menu. The circled numbers in Figure 2–10 refer to the step numbers in paragraph 2.4.4.1 that refers to that specific area of the display. The name of the display line is also included in each circle. By moving the cursor over any of these



PARAMETERS THAT MAY BE SELECTED FOR VIEWING					
BE	BER	BLK	BLE	EFB	EBR
TOD	MDY	ET	ED	ETS	ES
EFS	ESR	LOS	SLS	PF	ABE
ABER	CBE	CBER	EFS%	BITS	BLE%
BURS	PSL–	PSL+			

Figure 2–10. RS–232 BERT RESULTS/PARAMETERS Menu.

areas, it is possible to change that selected value just as if it were being accomplished on the BERT SETUP Menu.

For example, if the cursor were located over Ext Clk, pressing the CURSOR SELECT keys would change the bit rate selection to one of the values shown in Figure 2–7.

2. FRE JTR % – This line is used to display the results of the low speed (75 to 72000 bps) jitter measurements. The line displays four different readings (all as a percent of bit period).

   The 5500A uses a sampling technique to measure edge timing differences on the received data. The received data is sampled at approximately 250 times the bit rate. The result of this sample is used to synchronize an internal clock to the average data transitions. Edge jitter is then calculated by measuring the percent of difference between the actual transitions of the received data and the transitions of the synchronized internal clock.

   It should be noted that this sampling technique depends on transitions to achieve accuracy and synchronize the internal clock. Therefore, data with a 50% ratio of mark to spaces will result in the most accurate readings, while a long string of zero's would introduce errors.

   The four readings that appear on this line are:

pp Represents peak–to–peak or the largest differences in edges during 1024 samples at frequencies above 300 bps or 256 samples below 300 bps.

+ p Represents the largest difference in data edges that is later than the internal oscillator.

– p Represents the largest difference in data edges that is earlier than the internal oscillator.

av Represents the average difference between data edges, sampled over the same bit period as **pp**, **+ p**, and **– p**.

   The values that appear on this line will be numeric, 0–99, if the frequency of the receive data is between 75 and 72000 bps. If the receive data is outside the frequency range, a *na* will appear as the value.

   The only operator selection available on this line is **FRE** or **HLD**. The selection is made by placing the cursor over the first field in this line (FRE or HLD) and pressing either select key to toggle between FRE and HLD.

3. The measurement of the time interval between two specific events is required for some test applications. This line on the menu permits the user to select the events from the following; TD (transmit data), RD (receive data), CTS, RTS, DCD, DSR, DTR, or SQ and DLY (network loop delay). The network loop delay can measure on a single transmission (SNGL) or continuously (CONT). On the other measurements, the user may further select where the measurement is to take place; the leading or rising edge of the pulse (/) or the trailing or falling edge of the pulse (\). The time interval scale is the next item to set. This value is 1, 10, or 100 us, 1, 10, or 100 ms, or 1, 10, or 100 seconds. The numeric value in the field is then multiplied by the scale factor to obtain the time interval between the two events.

4. Frequency – This line is used to measure the frequency of the receive clock (RC), transmit clock (TC), external clock (XC), or the asynchronous bit rate (BR). The actual frequency being measured will appear in the field unless the frequency is below 150 Hz in which case the field will display UNDER.

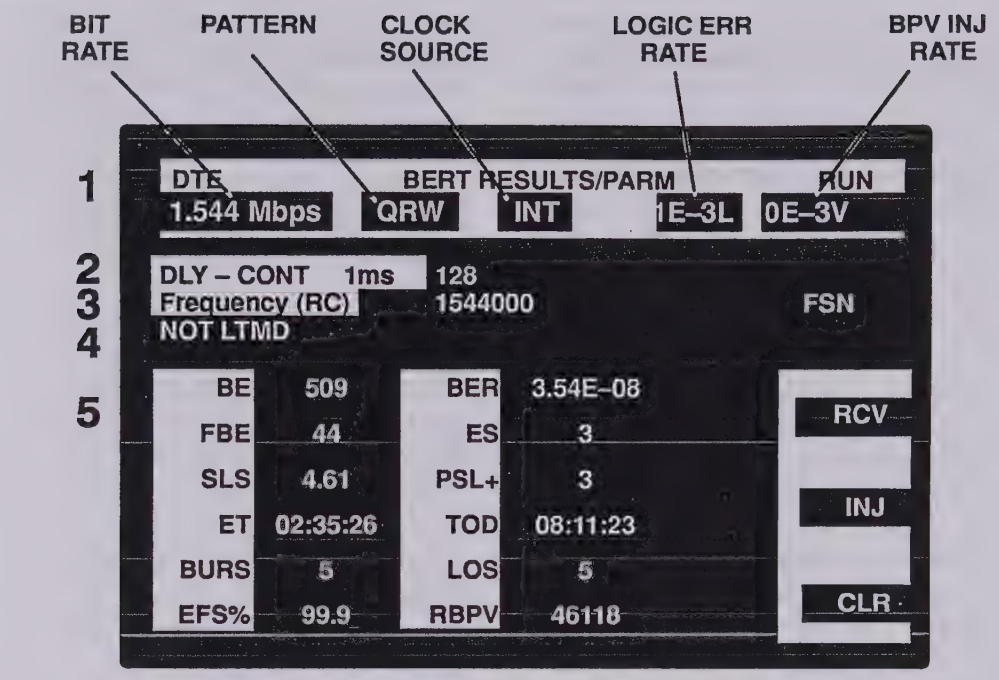
5. There are eight windows available to the user to display any eight of the parameters listed in Figure 2–10. The 5500A keeps track of all the parameters simultaneously and the user may scroll between any or all of them in these windows, at any time, without disrupting the test in progress.

2.4.5.2 FRACT T1 BERT RESULTS Menu

The three softkeys for this menu (Figure 2–11) perform the same functions as they do on the RS–232 BERT Results/Parameters menu and are explained in paragraph 2.4.5.1.

The FSN/FSL field above the softkey fields is **not** a softkey. FSN is displayed when the 5500A is in frame sync. FSL is displayed when frame sync is lost. FSN flashes when frame sync has been lost and then recovered.

1. The top line of this display identifies the menu, the selected termination mode, and if the 5500A is in the RUN mode. The second line is a condensed version of the FRACT T1 BERT SETUP Menu. The circled numbers in Figure 2–11 refer to the step numbers in paragraph 2.4.4.1 that refers to that specific area of the display. The name of the display line is also included in each circle. By moving the cursor over any of these areas, it is possible to change that selected value just as if it



PARAMETERS THAT MAY BE SELECTED FOR VIEWING

BE	BER	BLK	BLE	EFB	EBR	PSL+
TOD	MDY	ET	ED	ETS	ES	PSL–
EFS	ESR	LOS	SLS	PF	ABE	BLE%
ABER	CBE	CBER	RBPV	RVR	RVS	FFS%
RVFS	EFS%	%1sD	FLS	ALRM	AHST	CFS%
FBE	FBER	FBES	FEFS	CRCE	CRER	
CRES	CEFS	15Z	15ZS	FLOS	CSLP	
WND+	WND–	BALS	YALS	BITS	BURS	

Figure 2–11. FRAC T1 BERT RESULTS Menu.

were being accomplished on the FRACT T1 BERT SETUP Menu.

For example, if the cursor were located over clock source, pressing either of the **CURSOR SELECT** keys would change the CLOCK SOURCE selection to one of the seven available choices.

2. This line is used to display the network loop delay. Network loop delay is measured by sending a bit error from the 5500A through the network to the looped distant end. The 5500A measures the time it takes from initial transmission of the bit error to the return of the bit error to the 5500A and displays that total time as network loop delay. The network loop delay timer can measure times up to 17 minutes and can display the loop times in 1 usec, 10 usec, .1 Msec, 1 Msec, or 10 Msec resolution. (Refer to paragraph 2.6.2., Network Loop Timing.)

3. Frequency (RC) – This line is used to measure the frequency of receive clock (RC), transmit clock (TC), or external clock (XC). The actual frequency being measured will appear in the field unless the frequency is below 150 Hz in which case the field will display UNDER.

4. This line is used in conjunction with the clock slip (CLSP) measurement. As long as CLSP remains within the range of plus or minus 40 unit intervals, the LTMD (loop timed) indication will be displayed in this field. When CSLP exceeds this range, the flashing NOT LTMD (not loop timed) indication will appear in this field.

5. There are twelve windows available to the user to display any of the parameters listed in Figure 2–11. The 5500A keeps track of all the parameters simultaneously and the user may scroll between any or all of them in these windows, at any time, without disrupting the test in progress.

2.4.6 Printer Setup Menu

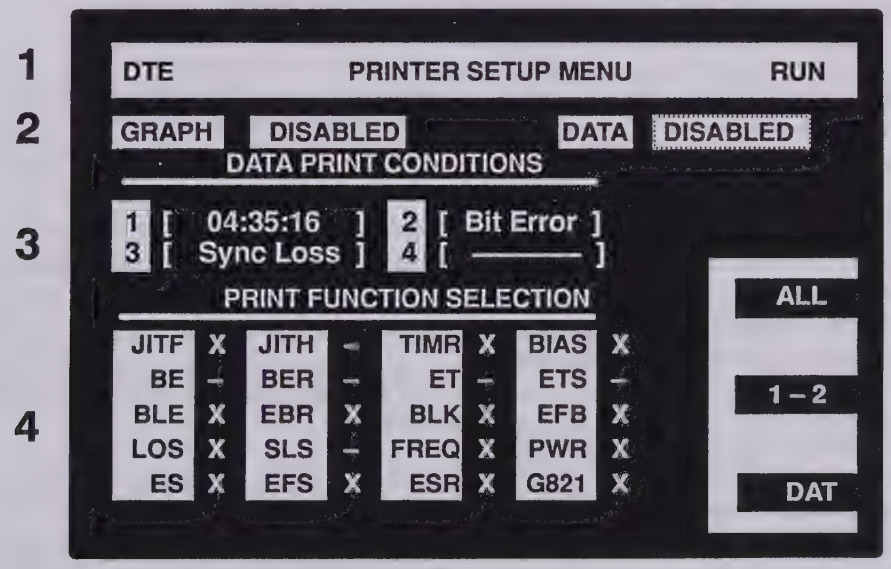
The Printer Setup Menus, illustrated in Figure 2–12 and Figure 2–13, are used in conjunction with an optional printer to provide the user with time and date stamped hard copy of test results. The only difference between the RS–232 Printer Setup Menu and the ESF T1 Printer Setup Menu, is the number of parameters available for printing and the conditions under which a printout can take place.

The softkeys for these menus are used to control what is to be printed. The top two keys, ALL and 1–2, are used when a graph is to be printed. Press the ALL softkey to command the printer to print the entire graph. Press the 1–2 softkey to instruct the printer to print only that section of the graph that appears between cursor #1 and cursor #2 (see paragraph 2.4.8 for information about the Graph Display). The final softkey, the DAT key, is used to instruct the printer to print the numeric data.

The explanation for each of the keyed areas in Figure 2–12 and Figure 2–13 follows:

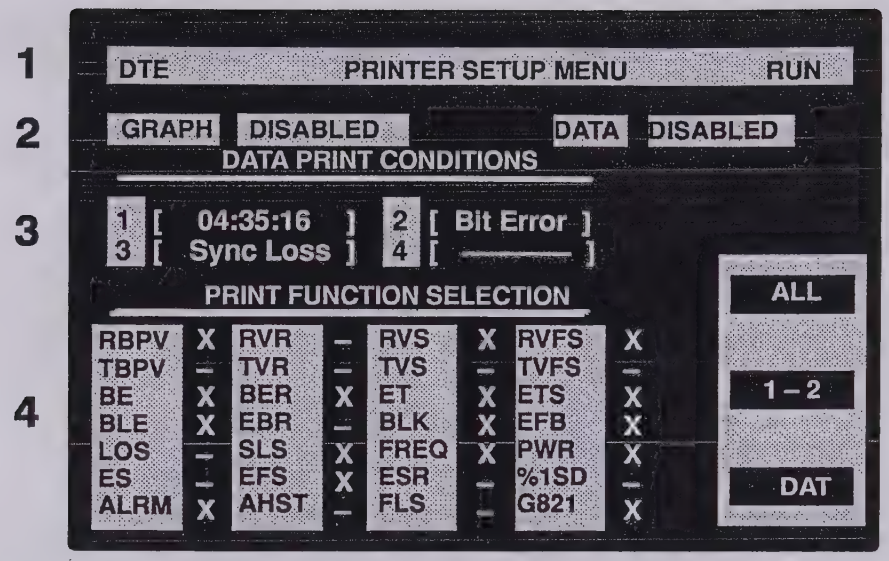
1. This line is the same as the previous menus.
2. This area of the display is used to ENABLE or DISABLE the graph printout functions. Place the cursor in the field to the right of GRAPH and use the CURSOR SELECT keys to select ENABLE or DISABLE.

   This area of the display is also used to ENABLE or DISABLE the data printout functions. Place the cursor in the field to the right of DATA and use the CURSOR SELECT keys to select ENABLE, ENB–ALRM, or DISABLE. The ENB–ALRM position sounds an audible alarm each time the print function is enabled.
3. This area of the menu, the DATA PRINT CONDITIONS, is used to select 1, 2, 3, or 4 conditions under which a print out will take place. In the example



DATA PRINT CONDITIONS
Err Sec, Sync Loss, Test End, Block, Blk Error, Bit Error, 24 hour, 12 hour, 6 hour,1 hour, 30 min, 15 min, 10 min, 5 min, 1 min, HH:MM:SS, ———

Figure 2–12. RS–232 PRINTER SETUP Menu.



DATA PRINT CONDITIONS
Err Sec, Sync Loss, Test End, Block, Blk Error, Bit Error, 24 hour, 12 hour, 6 hour, 1 hour, 30 min, 15 min, 10 min, 5 min, 1 min, HH:MM:SS, All Ones, All Zeros, 12.5% 1sD,T1 Alarms, BPV, ———

Figure 2–13. ESF T1 PRINTER SETUP Menu.

shown in Figure 2–13, a printout will occur every 4 hours, 35 minutes, and 16 seconds (line 1), every time there is a bit error (line 2), and every time there is a sync loss (line 3). The available print conditions are listed in Figure 2–12 and Figure 2–13. In addition to the pre–programmed times on which a printout will take place, the user may select any time period by using the HH:MM:SS format in one of the fields and entering the desired frequency for a printout in hours, minutes, and seconds.

4. This area of the display, the PRINT FUNCTION SELECTION, is used to select those parameters the user wishes to have on the printed results. An "X" after the parameter indicates the parameter has been selected to be printed. Selection is made by placing the cursor opposite the desired parameter, over the X or –, and using the CURSOR SELECT keys to enable (X) or disable (–) the printing of the parameter.

2.4.7 Graph Setup Menu

The Graph Setup Menu is shown in Figure 2–14. The softkeys for this menu are used to change the previous graph data selection to the current selection. The SELECT softkey will activate any changes that have been made on this menu and discard any stored graph data while the CANCEL softkey will cancel any changes that have been made without discarding the stored graph data. The softkey labels (SELECT and CANCEL) will flash to indicate that the stored configuration and the graph data do not match the displayed configuration.

The explanation for each of the keyed areas in Figure 2–14 follows:

1. The top line of the display is the same as in previous menus.
2. The SAMPLE PERIOD field defines the sample resolution for the stored graph data. The resolutions available are 1 second, 10 seconds, 1 minute, 10 minutes, and 1 hour. Graph data can then be displayed at the selected period or the next 2 resolutions (selection is made on the Graph Display Menu, paragraph 2.4.8).
3. The PRINT RESOLUTION field defines the resolution of the printed graph data. The graph can be printed at

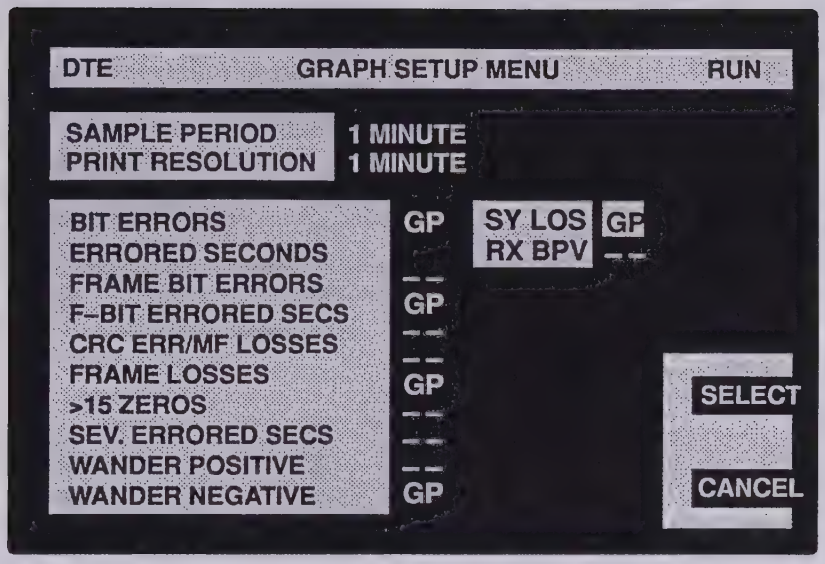


Figure 2–14. GRAPH SETUP Menu.

the sample period or the next two resolutions as summarized below:

Sample Resolution	Print Period
1 second	1 or 10 seconds
	1 minute
10 seconds	10 seconds
	1 or 10 minutes
1 minute	1 or 10 minutes
	1 hour
10 minutes	10 minutes
	1 hour
1 hour	1 hour

4. The parameter field permits the user to select the parameter(s) to be graphed (G), graphed and printed (GP) or not selected for either (—). Selection is made by placing the cursor opposite the desired parameter and using the CURSOR SELECT keys to choose G, GP, or —.

2.4.8 GRAPH Display

The GRAPH SETUP Display located to the left of the BERT DISPLAY in the menu matrix provides the user with an important tool in locating the source of a problem.

Often, the cause of a burst of errors may be related to its time occurrence. That is, a large air conditioner or other high power device may cycle on and the surge may cause a nearby terminal or modem to suffer a power line hit. The events can be correlated to the cause using the GRAPH DISPLAY.

The operator may choose to plot up to four different error parameters versus time so as to generate a more complete picture of circuit conditions.

A typical graph display of bit errors is shown in Figure 2–15. A typical test setup might involve graphing bit errors, sync losses, bipolar violations (T–Carrier testing), and errored blocks. Other parameters can be graphed, however, the above are the most important in isolating problems.

The Graph Display stores up to 90 hours of data in up to one minute intervals if only one parameter is graphed. This permits long term unattended testing (over a weekend for example) without losing the data, or when it occurred. The Graph Display storage time is dependent on the total number of parameters and the sample time. The maximum sampling time is achieved when sampling 1 parameter at one sample per hour. The total amount of storage time for this example is 5400 hours.

When setting up a GRAPH DISPLAY for a long term test, it is suggested to set the HORIZONTAL time scale to sixty minutes per division and the VERTICAL scale to x1 for the maximum sensitivity. This will cause even single events to be displayed. When the user wishes to view the display the scales can always be changed for a more convenient display. No data is lost by changing the scales.

The user also can print out the graphic data (for a single parameter). The 5500A will print out data continuously in 1, 10, or 60 minute increments depending upon the horizontal

scale setting. The user can therefore bypass the 60 hour limitation of the GRAPH DISPLAY itself.

Figure 2–14 and Figure 2–15 detail the setup for graph data (GRAPH DATA SELECTION). Figure 2–15 details the actual graph display and display controls. This menu does not have any softkeys associated with the display. Table 2–5 presents the graph definitions. The 5500A graph is provided only under local control. For remote control operation, an intelligent controller may be utilized to obtain data plots.

The explanation for each of the keyed areas in Figure 2–15 follows:

1. The top line of this display is different in that the title of the menu does not appear in the top center. Instead, the top center of this menu is used to display the parameter being graphed from the list of those selected on the Graph Data Selection menu. Select the parameter to view by positioning the cursor over the function displayed (at the top of the display) and then use the CURSOR SELECT keys to scroll to the desired

Parameters That Can Be Viewed in Fields Above Mag1							
WITH RS–232 MODULE INSTALLED				WITH ESF T1 MODULE INSTALLED			
BITS	EFS%	CBER	CBE	ALL OF THE PARAMETERS LISTED ON LEFT PLUS:			
ABER	ABE	PF	SLS				
LOS	ESR	EFS	ES				
ETS	ED	ET	MDY	YALS	BALS	WND–	WND+
TOD	EBR	EFB	BLE	CSLP	FLOS	15ZS	15Z
BLK	BER	BE		CEFS	CRES	CRER	CRCE
				FEFS	FBES	FBER	FBE
				AHST	ALRM	FLS	%1sD
				RVFS	RVS	RVR	RBPV

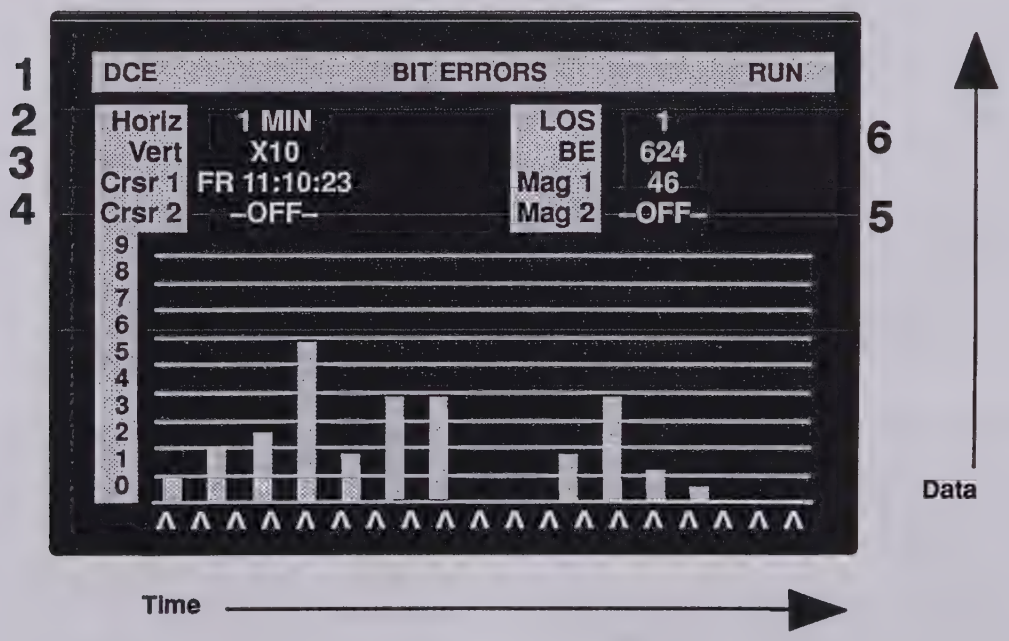


Figure 2–15. Graph Display.

parameter. The remaining top line fields are the same as in previous displays.

2. The Horiz field is used to select the time scale factor based upon the SAMPLE PERIOD selection made on the Graph Data Selection Menu.

Table 2–5. Graph Definitions.

SYMBOL	DEFINITION
Crsr 1	The main cursor for the graph used to determine the exact time and magnitude of the data being plotted. The UP SELECT key advances the cursor in the time increments set by the horizontal resolution. The DOWN SELECT key backs up the cursor in time. A time of day clock reading is provided next to the Crsr 1 display.
Crsr 2	Cursor 2 is used for the plot printing function. Data between Cursor 1 and Cursor 2 can be printed out by depressing the SOFTKEY corresponding to 1–2 in the PRINT SELECTION Menu.
Horizontal (Horiz)	CRT field that displays the time scale selected. One, ten or sixty minutes per division may be selected. Thirty time divisions can be displayed without scrolling to the right. The resolution decreases as the number of parameters to be graphed increases.
Vertical (Vert)	CRT field that displays the vertical scale factor. Factors from 1 to 100,000 are provided.
Mag 1	Displays the magnitude of the data at Cursor 1 position.
Mag 2	Displays the magnitude of the data at Cursor 2 position.
ALL	Softkey used to print entire sixty hour graph plot. Will also enable continuous printout of graph data.
1–2	Prints graph data between Cursor 1 and 2 only.
DAT	Softkey used to select numerical data print out instead of graphic data. Used with any standard RS–232 interface printer.
Top Line Center of graph display	CRT field used to select data parameter(s) to be plotted.

NOTE The graph data buffer is approximately 5400 samples long. Data is collected and stored until the buffer is full. The oldest samples are discarded as required to make room for new samples. The period of time that is represented by data in the buffer is a function of the sample period and the number of data types to be sampled. For example, assume the sample period is 10 seconds with three data types selected. To compute buffer length:

Buffer length = (5400/3)*10 = 18,000 seconds = 5 hours

3. The Vert field selects the vertical resolution for the displayed graph. The vertical resolution selects a magnitude multiplier corresponding to the labels on the left side of the display.

4. The Crsr 1 and Crsr 2 define the day–of–the–week, hour, and minute of the samples at cursors 1 and 2. The two cursors may be used to print a section of the graph data. Cursor 2 may be off. If not, cursor 1 always precedes cursor 2.

5. The Mag 1 and Mag 2 fields display the magnitude of the data at cursors 1 and 2.

6. The two fields above the Mag 1 field are used to display the numeric results of a selected parameter (these parameters are not controlled by the parameters on the Graph Data Selection Menu). To select the desired parameter, move the cursor to either field and use the CURSOR SELECT keys to select the desired parameter. The available parameters are listed in Figure 2–15.

2.4.9 RS–232/IEEE–488 Menu

The RS–232/IEEE–488 Menu, illustrated in Figure 2–16, is used to configure the 5500A remote ports to match the device to be connected to the port, ie., a printer or terminal.

NOTE A detailed explanation of the RS–232 IEEE–488 menu is located in the Remote Operations section of this manual.

The softkeys for this menu are used to select RS–232, IEEE–488, or PRINTER. If RS–232 operation is going to be used, the user presses the RS–232 softkey if a terminal or modem is to be connected to the 5500A RS–232 remote port. If a direct printer connection is to be made via the RS–232 remote port, the PRINTER softkey is pressed. When the parallel IEEE–488 (sometimes referred to as GPIB or HPIB) remote port is to be used, the IEEE–488 softkey is pressed.

NOTE To change gender of the remote port, the switches on the control board must be changed.

The explanation for each of the keyed areas in Figure 2–16 follows:

1. The TRACE field is used to view the character stream between the 5500A and the remote device over the remote port for possible trouble–shooting. When the TRACE is ENABLED, the user will observe the data stream going to the remote device on the right half of the line and the data stream coming from the remote device on the left side of this line of the display. The trace will also be visible on all the other menus that have the trace brackets "] [" on the second line of the display.
2. The PROTOCOL field is used to select the controller response format. The choices are CR–LF and ACK–NAK.
3. This area of the menu is used to select the various RS–232 protocols. The bit rate is selectable from 50, 75, 110, 150, 300, 600, 1200, 2400, 4800, 7200, 9600, or 19200 bps. The character size may be 7 or 8 bits, parity of odd, even, or none, and stop bits of 1, 1.5, or 2. These are all selected by placing the cursor over the selected field and using the CURSOR SELECT keys to scroll to the desired value.
4. The IEEE–488 bus enables the simultaneous connection of up to 31 devices to a single controller. Each device on the bus has a numeric address (0–30). It is therefore necessary to "tell" the 5500A what its

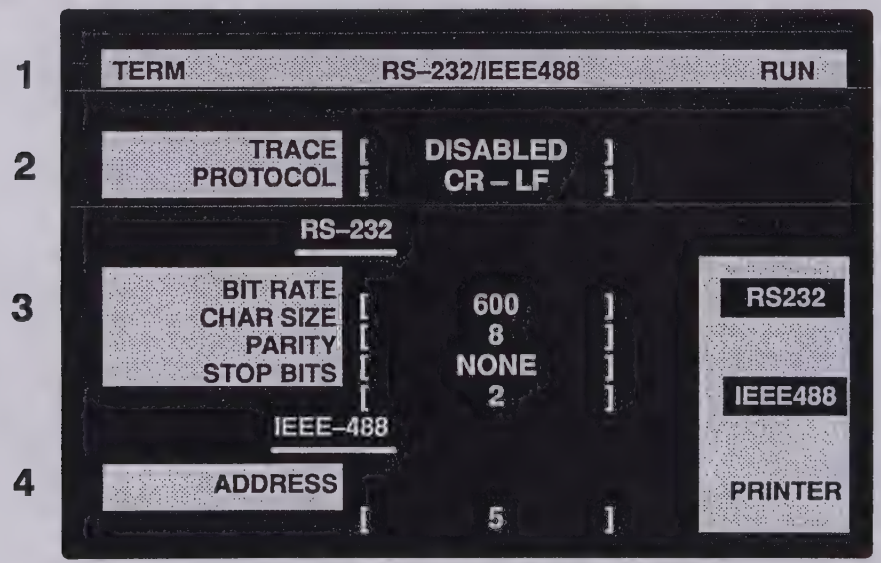


Figure 2–16. RS 232/IEEE488 Menu.

address is so that it will respond to information sent to it. This line is used to set that address into the 5500A. Place the cursor over the address field and use the front panel keypad or select keys to enter the address.

2.4.10 STORE/RECALL SETUPS Menu

The STORE/RECALL SETUPS Menu, illustrated in Figure 2–17, is used to store up to ten complete configuration setups, thus making it much faster to repeat a recurring test at a later date.

The softkeys for this menu are used to store (STR), recall (RCL), or clear (CLR) a program area. The STR softkey stores the current setup in the memory location indicated by the cursor. The RCL softkey recalls the setup configuration stored in the memory location indicated by the cursor. The CLR softkey clears the program name from the menu field for the selected memory location, but does not clear the memory location of the configuration setup.The front panel STORE and RECALL keys work in the same manner as the softkeys on this menu. To store a configuration into memory, follow these simple steps:

a. Setup the 5500A for the test desired.

b. Press the STORE key.

c. Press the keypad number for the memory location into which this setup is to be stored. (The user may overwrite any previously stored configuration by simply storing a new configuration in the old location.)

d. Name the program following the procedure in #1 below.

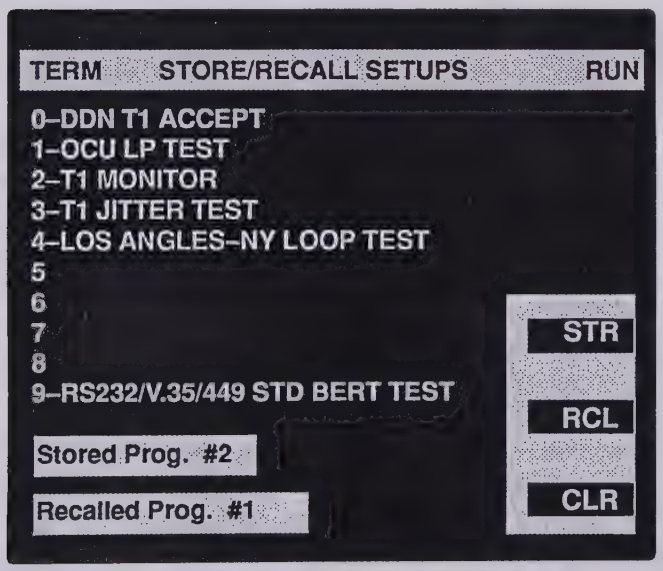


Figure 2–17. STORE/RECALL SETUPS Menu.

To recall a program, follow these steps:

a. Press the RECALL key twice within 2 seconds.

b. Enter the number of the desired program using the front panel keypad.

The explanation for each of the keyed areas in Figure 2–17 follows:

1. The fields numbered 0 – 9 represent memory locations in which a particular configuration setup may be stored by the user. The field opposite the number is provided so that the user may assign a name to the program for ease in identification. The name may be typed in using a terminal or by placing the cursor over the character position and then use the CURSOR SELECT keys to scroll through the character set until the desired character is in place.
2. The Stored Prog field displays the number of the most recent program stored by the user.
3. The Recalled Prog field displays the number of the most recent program recalled by the user.

2.4.11 USER PATTERN Menu

The USER PATTERN Menu, Figure 2–18, allows the user to construct patterns for transmission by the 5500A. The USER PATTERN selection, when chosen, causes the 5500A to transmit a repetitive pattern of whatever the operator has placed in the USER PATTERN display. The user is permitted to enter up to 135 characters (2200 in User pattern 4) in HEX from the front panel HEX keypad or over the remote control ports. Each character in HEX is an 8 bit long word so the total bit length which could be input is 1080 bits. However, the user may enter as few as three characters if desired. When using unframed modules, the first three bytes of the user pattern must be unique to the rest of the user pattern to avoid false sync detects. The pattern is transmitted LSB first (i.e., 80H is transmitted 0000 0001).

When utilizing 624/628/636/828/836 modules, the user pattern sync mode may be set to OFF, FRAME, or SUPER FRM. These user pattern sync modes are provided for those test applications where the user must be able to control the bit patterns in specific channel time slots of the T1/CEPT signal. For example, an examination of the T1 bit

alignment reveals that the frame mode will align a 24 byte user data pattern with T1 frame sync so that byte one of the user pattern is transmitted in the first time slot of the framed T1 signal, byte two is in the second time slot, and so on. However, the superframe mode will align a 288 byte D4 or SLC®96 framed pattern or 576 byte ESF framed pattern to the pattern start. The first 24 bytes go out in frame one of a superframe, the second 24 bytes go out in frame two, etc.

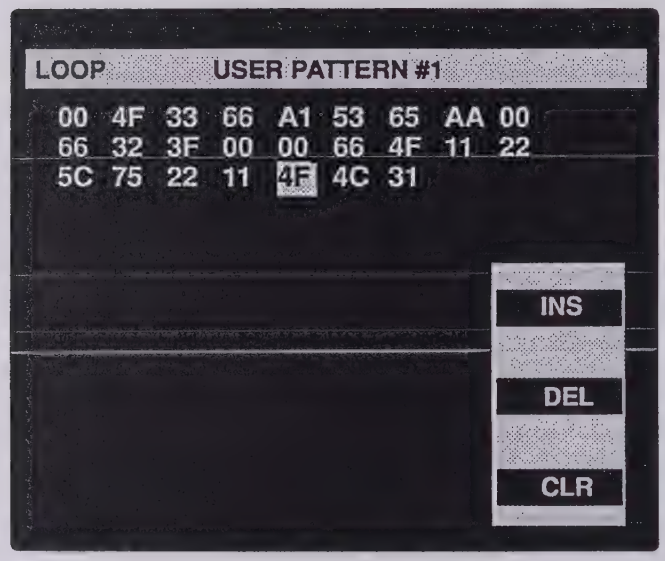


Figure 2–18. USER PATTERN Menu.

Because of the length of a superframe, USER PATTERN #4 must be used. Also note that the three unique bytes must appear in bytes four, five, and six instead of one, two, and three running unframed. This will avoid false sync detects and ensure proper frame alignment.

NOTE If the RAM backup battery failed or has been replaced, it is possible that the 5500A will power up, default to the System Menu, and flash the USER PATTERN "Invalid" memory block. This "error" can be ignored or the user may choose to place three or four characters into the User Pattern display. These can be any HEX characters or the user may want to place an actual pattern into memory.

The user may desire to input a pattern on a binary, bit–by–bit basis. This is a somewhat more complex procedure, but the following table and examples will serve to explain the procedure.

Tables 2–6 through 2–13 provide universal translation codes for HEX to 7–Bit ASCII No Parity, HEX to 8–Bit ASCII Even Parity, HEX to 8–Bit ASCII Odd Parity, HEX to 8–Bit Mark Parity, HEX to EBCDIC, HEX to BAUDOT, HEX to Binary Conversion, and a miscellaneous chart for universal combinations.

Table 2–6. HEX to 7–Bit ASCII No Parity.

HEX	CHAR	TYPE	HEX	CHAR	HEX	CHAR	HEX	CHAR
00	NUL	–	20	space	40	@	60	'
01	SOH	CTRL–A	21	!	41	A	61	a
02	STX	CTRL–B	22	"	42	B	62	b
03	ETX	CTRL–C	23	#	43	C	63	c
04	EOT	CTRL–D	24	$	44	D	64	d
05	ENQ	CTRL–E	25	%	45	E	65	e
06	ACK	CTRL–F	26	&	46	F	66	f
07	BEL	CTRL–G	27	'	47	G	67	g
08	BS	CTRL–H	28	(	48	H	68	h
09	TAB	CTRL–I	29	)	49	I	69	i
0A	LF	CTRL–J	2A	*	4A	J	6A	j
0B	VT	CTRL–K	2B	+	4B	K	6B	k
0C	FF	CTRL–L	2C	,	4C	L	6C	l
0D	CR	CTRL–M	2D	–	4D	M	6D	m
0E	SO	CTRL–N	2E	.	4E	N	6E	n
0F	SI	CTRL–O	2F	/	4F	O	6F	o
10	DLE	CTRL–P	30	0	50	P	70	p
11	DC1	CTRL–Q	31	1	51	Q	71	q
12	DC2	CTRL–R	32	2	52	R	72	r
13	DC3	CTRL–S	33	3	53	S	73	s
14	DC4	CTRL–T	34	4	54	T	74	t
15	NAK	CTRL–U	35	5	55	U	75	u
16	SYN	CTRL–V	36	6	56	V	76	v
17	ETB	CTRL–W	37	7	57	W	77	w
18	CAN	CTRL–X	38	8	58	X	78	x
19	EM	CTRL–Y	39	9	59	Y	79	y
1A	SUB	CTRL–Z	3A	:	5A	Z	7A	z
1B	ESC	ESC	3B	;	5B	[	7B	{
1C	FS	–	3C	<	5C	\	7C	:
1D	GS	–	3D	=	5D	]	7D	}
1E	RS	–	3E	>	5E	^	7E	~
1F	US	–	3F	?	5F	<–	7F	DEL

Table 2–7. HEX to 8–Bit ASCII Even Parity.

HEX	CHAR	TYPE	HEX	CHAR	HEX	CHAR	HEX	CHAR
00	NUL	–	A0	space	C0	@	60	'
81	SOH	CTRL–A	21	!	41	A	E1	a
82	STX	CTRL–B	22	"	42	B	E2	b
03	ETX	CTRL–C	A3	#	C3	C	63	c
84	EOT	CTRL–D	24	$	44	D	E4	d
05	ENQ	CTRL–E	A5	%	C5	E	65	e
06	ACK	CTRL–F	A6	&	C6	F	66	f
87	BEL	CTRL–G	27	'	47	G	E7	g
88	BS	CTRL–H	28	(	48	H	E8	h
09	TAB	CTRL–I	A9	)	C9	I	69	i
0A	LF	CTRL–J	AA	*	CA	J	6A	j
8B	VT	CTRL–K	2B	+	4B	K	EB	k
0C	FF	CTRL–L	AC	,	CC	L	6C	l
8D	CR	CTRL–M	2D	–	4D	M	ED	m
8E	SO	CTRL–N	2E	.	4E	N	EE	n
0F	SI	CTRL–O	AF	/	CF	O	6F	o
90	DLE	CTRL–P	30	0	50	P	F0	p
11	DC1	CTRL–Q	B1	1	D1	Q	71	q
12	DC2	CTRL–R	B2	2	D2	R	72	r
93	DC3	CTRL–S	33	3	53	S	F3	s
14	DC4	CTRL–T	B4	4	D4	T	74	t
95	NAK	CTRL–U	35	5	55	U	F5	u
96	SYN	CTRL–V	36	6	56	V	F6	v
17	ETB	CTRL–W	B7	7	D7	W	77	w
18	CAN	CTRL–X	B8	8	D8	X	78	x
99	EM	CTRL–Y	39	9	59	Y	F9	y
9A	SUB	CTRL–Z	3A	:	5A	Z	FA	z
1B	ESC	ESC	BB	;	DB	[	7B	{
9C	FS	–	3C	<	5C	\	FC	:
1D	GS	–	BD	=	DD	]	7D	}
1E	RS	–	BE	>	DE	^	7E	~
9F	US	–	3F	?	5F	<–	FF	DEL

Table 2–8. Hex to 8–Bit ASCII Odd Parity.

HEX	CHAR	TYPE	HEX	CHAR	HEX	CHAR	HEX	CHAR
80	NUL	–	20	space	40	@	E0	'
01	SOH	CTRL–A	A1	!	C1	A	61	a
02	STX	CTRL–B	A2	"	C2	B	62	b
83	ETX	CTRL–C	23	#	43	C	E3	c
04	EOT	CTRL–D	A4	$	C4	D	64	d
85	ENQ	CTRL–E	25	%	45	E	E5	e
86	ACK	CTRL–F	26	&	46	F	E6	f
07	BEL	CTRL–G	A7	'	C7	G	67	g
08	BS	CTRL–H	A8	(	C8	H	68	h
89	TAB	CTRL–I	29	)	49	I	E9	i
8A	LF	CTRL–J	2A	*	4A	J	EA	j
0B	VT	CTRL–K	AB	+	CB	K	6B	k
8C	FF	CTRL–L	2C	,	4C	L	EC	l
0D	CR	CTRL–M	AD	–	CD	M	6D	m
0E	SO	CTRL–N	AE	.	CE	N	6E	n
8F	SI	CTRL–O	2F	/	4F	O	EF	o
10	DLE	CTRL–P	B0	0	D0	P	70	p
91	DC1	CTRL–Q	31	1	51	Q	F1	q
92	DC2	CTRL–R	32	2	52	R	F2	r
13	DC3	CTRL–S	B3	3	D3	S	73	s
94	DC4	CTRL–T	34	4	54	T	F4	t
15	NAK	CTRL–U	B5	5	D5	U	75	u
16	SYN	CTRL–V	B6	6	D6	V	76	v
97	ETB	CTRL–W	37	7	57	W	F7	w
98	CAN	CTRL–X	38	8	58	X	F8	x
19	EM	CTRL–Y	B9	9	D9	Y	79	y
1A	SUB	CTRL–Z	BA	:	DA	Z	7A	z
9B	ESC	ESC	3B	;	5B	[	FB	{
1C	FS	–	BC	<	DC	\	7C	B
9D	GS	–	3D	=	5D	]	FD	}
9E	RS	–	3E	>	5E	^	FE	~
1F	US	–	BF	?	DF	z	7F	DEL

Table 2–9. Hex to 8–Bit ASCII Mark Parity.

HEX	CHAR	TYPE	HEX	CHAR	HEX	CHAR	HEX	CHAR
80	NUL	–	A0	space	C0	@	E0	'
81	SOH	CTRL–A	A1	!	C1	A	E1	a
82	STX	CTRL–B	A2	"	C2	B	E2	b
83	ETX	CTRL–C	A3	#	C3	C	E3	c
84	EOT	CTRL–D	A4	$	C4	D	E4	d
85	ENQ	CTRL–E	A5	%	C5	E	E5	e
86	ACK	CTRL–F	A6	&	C6	F	E6	f
87	BEL	CTRL–G	A7	'	C7	G	E7	g
88	BS	CTRL–H	A8	(	C8	H	E8	h
89	TAB	CTRL–I	A9	)	C9	I	E9	i
8A	LF	CTRL–J	AA	*	CA	J	EA	j
8B	VT	CTRL–K	AB	+	CB	K	EB	k
8C	FF	CTRL–L	AC	,	CC	L	EC	l
8D	CR	CTRL–M	AD	–	CD	M	ED	m
8E	SO	CTRL–N	AE	.	CE	N	EE	n
8F	SI	CTRL–O	AF	/	CF	O	EF	o
90	DLE	CTRL–P	B0	0	D0	P	F0	p
91	DC1	CTRL–Q	B1	1	D1	Q	F1	q
92	DC2	CTRL–R	B2	2	D2	R	F2	r
93	DC3	CTRL–S	B3	3	D3	S	F3	s
94	DC4	CTRL–T	B4	4	D4	T	F4	t
95	NAK	CTRL–U	B5	5	D5	U	F5	u
96	SYN	CTRL–V	B6	6	D6	V	F6	v
97	ETB	CTRL–W	B7	7	D7	W	F7	w
98	CAN	CTRL–X	B8	8	D8	X	F8	x
99	EM	CTRL–Y	B9	9	D9	Y	F9	y
9A	SUB	CTRL–Z	BA	:	DA	Z	FA	z
9B	ESC	ESC	BB	;	DB	[	FB	{
9C	FS	–	BC	<	DC	\	FC	B
9D	GS	–	BD	=	DD	]	FD	}
9E	RS	–	BE	>	DE	^	FE	~
9F	US	–	BF	?	DF	z	FF	DEL

Table 2–10. Hex – EBCDIC.

HEX	CHAR	HEX	CHAR	HEX	CHAR	HEX	CHAR
00	NUL	40	space	7C	@	79	'
01	SOH	5A	!	C1	A	81	a
02	STX	7F	"	C2	B	82	b
03	ETX	7B	#	C3	C	83	c
37	EOT	5B	$	C4	D	84	d
2D	ENQ	6C	%	C5	E	85	e
2E	ACK	50	&	C6	F	86	f
2F	BEL	7D	'	C7	G	87	g
16	BS	4D	(	C8	H	88	h
05	TAB	5D	)	C9	I	89	i
25	LF	5C	*	D1	J	91	j
0B	VT	4E	+	D2	K	92	k
0C	FF	6B	,	D3	L	93	l
0D	CR	60	-	D4	M	94	m
0E	SO	4B	.	D5	N	95	n
0F	SI	61	/	D6	O	96	o
10	DLE	F0	0	D7	P	97	p
11	DC1	F1	1	D8	Q	98	q
12	DC2	F2	2	D9	R	99	r
13	DC3	F3	3	E2	S	A2	s
3C	DC4	F4	4	E3	T	A3	t
3D	NAK	F5	5	E4	U	A4	u
32	SYN	F6	6	E5	V	A5	v
26	ETB	F7	7	E6	W	A6	w
18	CAN	F8	8	E7	X	A7	x
19	EM	F9	9	E8	Y	A8	y
3F	SUB	7A	:	E9	Z	A9	z
27	ESC	5E	;		[	C0	{
22	FS	4C	<	E0	\	6A	|
		7E	=		]	D0	}
35	RS	6E	>		^	A1	~
		6F	?	6D	_	07	DEL

Table 2–11. Hex to BAUDOT.

HEX	LETTERS CHAR	FIGURES CHAR	TYPE
18	A	-	
13	B	?	
0E	C	:	
12	D	$	
10	E	3	
16	F	!	
0B	G	&	
05	H	#	
0C	I	8	
1A	J	BELL	
1E	K	(	
09	L	)	
07	M	.	
06	N	,	
03	O	9	
0D	P	0	
1D	Q	1	
0A	R	4	
14	S	'	
01	T	5	
1C	U	7	
0F	V	;	
19	W	2	
17	X	/	
15	Y	6	
11	Z	"	
00			BLANK
1F			LETTERS SHIFT
1B			FIGURES SHIFT
04			SPACE
02			CARRIAGE RET
08			LINE FEED

Table 2–12. HEX to Binary Conversion.

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
00	00000000	50	00001010	A0	00000101
01	10000000	51	10001010	A1	10000101
02	01000000	52	01001010	A2	01000101
03	11000000	53	11001010	A3	11000101
04	00100000	54	00101010	A4	00100101
05	10100000	55	10101010	A5	10100101
06	01100000	56	01101010	A6	01100101
07	11100000	57	11101010	A7	11100101
08	00010000	58	00011010	A8	00010101
09	10010000	59	10011010	A9	10010101
0A	01010000	5A	01011010	AA	01010101
0B	11010000	5B	11011010	AB	11010101
0C	00110000	5C	00111010	AC	00110101
0D	10110000	5D	10111010	AD	10110101
0E	01110000	5E	01111010	AE	01110101
0F	11110000	5F	11111010	AF	11110101
10	00001000	60	00000110	B0	00001101
11	10001000	61	10000110	B1	10001101
12	01001000	62	01000110	B2	01001101
13	11001000	63	11000110	B3	11001101
14	00101000	64	00100110	B4	00101101
15	10101000	65	10100110	B5	10101101
16	01101000	66	01100110	B6	01101101
17	11101000	67	11100110	B7	11101101
18	00011000	68	00010110	B8	00011101
19	10011000	69	10010110	B9	10011101
1A	01011000	6A	01010110	BA	01011101
1B	11011000	6B	11010110	BB	11011101
1C	00111000	6C	00110110	BC	00111101
1D	10111000	6D	10110110	BD	10111101
1E	01111000	6E	01110110	BE	01111101
1F	11111000	6F	11110110	BF	11111101
20	00000100	70	00001110	C0	00000011
21	10000100	71	10001110	C1	10000011
22	01000100	72	01001110	C2	01000011
23	11000100	73	11001110	C3	11000011
24	00100100	74	00101110	C4	00100011
25	10100100	75	10101110	C5	10100011
26	01100100	76	01101110	C6	01100011
27	11100100	77	11101110	C7	11100011
28	00010100	78	00011110	C8	00010011
29	10010100	79	10011110	C9	10010011
2A	01010100	7A	01011110	CA	01010011
2B	11010100	7B	11011110	CB	11010011
2C	00110100	7C	00111110	CC	00110011
2D	10110100	7D	10111110	CD	10110011
2E	01110100	7E	01111110	CE	01110011
2F	11110100	7F	11111110	CF	11110011

Table 2–12. Hex to Binary Conversion (Cont.).

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
30	00001100	80	00000001	D0	00001011
31	10001100	81	10000001	D1	10001011
32	01001100	82	01000001	D2	01001011
33	11001100	83	11000001	D3	11001011
34	00101100	84	00100001	D4	00101011
35	10101100	85	10100001	D5	10101011
36	01101100	86	01100001	D6	01101011
37	11101100	87	11100001	D7	11101011
38	00011100	88	00010001	D8	00011011
39	10011100	89	10010001	D9	10011011
3A	01011100	8A	01010001	DA	01011011
3B	11011100	8B	11010001	DB	11011011
3C	00111100	8C	00110001	DC	00111011
3D	10111100	8D	10110001	DD	10111011
3E	01111100	8E	01110001	DE	01111011
3F	11111100	8F	11110001	DF	11111011
40	00000010	90	00001001	E0	00000111
41	10000010	91	10001001	E1	10000111
42	01000010	92	01001001	E2	01000111
43	11000010	93	11001001	E3	11000111
44	00100010	94	00101001	E4	00100111
45	10100010	95	10101001	E5	10100111
46	01100010	96	01101001	E6	01100111
47	11100010	97	11101001	E7	11100111
48	00010010	98	00011001	E8	00010111
49	10010010	99	10011001	E9	10010111
4A	01010010	9A	01011001	EA	01010111
4B	11010010	9B	11011001	EB	11010111
4C	00110010	9C	00111001	EC	00110111
4D	10110010	9D	10111001	ED	10110111
4E	01110010	9E	01111001	EE	01110111
4F	11110010	9F	11111001	EF	11110111
F0	00001111	F6	01101111	FB	11011111
F1	10001111	F7	11101111	FC	00111111
F2	01001111	F8	00011111	FD	10111111
F3	11001111	F9	10011111	FE	01111111
F4	00101111	FA	01011111	FF	11111111
F5	10101111				

Table 2–13. Universal Code Translation.

Dec.	Hex	Instruction (RR)	Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
0	00			NUL	NUL		12-0-1-8-9	0000 0000
1	01			SOH	SOH		12-1-9	0000 0001
2	02			STX	STX		12-2-9	0000 0010
3	03			ETX	ETX		12-3-9	0000 0011
4	04	SPM		PF	EOT		12-4-9	0000 0100
5	05	BALR		HT	ENQ		12-5-9	0000 0101
6	06	BCTR		LC	ACK		12-6-9	0000 0110
7	07	BCR		DEL	BEL		12-7-9	0000 0111
8	08	SSK		GE	BS		12-8-9	0000 1000
9	09	ISK		RLF	HT		12-1-8-9	0000 1001
10	0A	SVC		SMM	LF		12-2-8-9	0000 1010
11	0B			VT	VT		12-3-8-9	0000 1011
12	0C			FF	FF		12-4-8-9	0000 1100
13	0D			CR	CR		12-5-8-9	0000 1101
14	0E	MVCL		SO	SO		12-6-8-9	0000 1110
15	0F	CLCL		SI	SI		12-7-8-9	0000 1111
16	10	LPR		DLE	DLE		12-11-1-8-9	0001 0000
17	11	LNR		DC1	DC1		11-1-9	0001 0001
18	12	LTR		DC2	DC2		11-2-9	0001 0010
19	13	LCR		TM	DC3		11-3-9	0001 0011
20	14	NR		RES	DC4		11-4-9	0001 0100
21	15	CLR		NL	NAK		11-5-9	0001 0101
22	16	OR		BS	SYN		11-6-9	0001 0110
23	17	XR		IL	ETB		11-7-9	0001 0111
24	18	LR		CAN	CAN		11-8-9	0001 1000
25	19	CR		EM	EM		11-1-8-9	0001 1001
26	1A	AR		CC	SUB		11-2-8-9	0001 1010
27	1B	SR		CU1	ESC		11-3-8-9	0001 1011
28	1C	MR		IFS	FS		11-4-8-9	0001 1100
29	1D	DR		IGS	GS		11-5-8-9	0001 1101
30	1E	ALR		IRS	RS		11-6-8-9	0001 1110
31	1F	SLR		IUS	US		11-7-8-9	0001 1111
32	20	LPDR		DS	SP		11-0-1-8-9	0010 0000
33	21	LNDR		SOS	!	!	0-1-9	0010 0001
34	22	LTDR		FS	"		0-2-9	0010 0010
35	23	LCDR			#		0-3-9	0010 0011
36	24	HDR		BYP	$		0-4-9	0010 0100
37	25	LRDR		LF	%		0-5-9	0010 0101
38	26	MXR		ETB	&		0-6-9	0010 0110
39	27	MXDR		ESC	'		0-7-9	0010 0111
40	28	LDR			(		0-8-9	0010 1000
41	29	CDR			)		0-1-8-9	0010 1001
42	2A	ADR		SM	*		0-2-8-9	0010 1010
43	2B	SDR		CU2	+		0-3-8-9	0010 1011
44	2C	MDR			,		0-4-8-9	0010 1100
45	2D	DDR		ENQ	-		0-5-8-9	0010 1101
46	2E	AWR		ACK	.		0-6-8-9	0010 1110
47	2F	SWR		BEL	/		0-7-8-9	0010 1111
48	30	LPER			0		12-11-0-1-8-9	0011 0000
49	31	LNER			1		1-9	0011 0001
50	32	LTER		SYN	2		2-9	0011 0010
51	33	LCER			3		3-9	0011 0011
52	34	HER		PN	4		4-9	0011 0100
53	35	LRER		RS	5		5-9	0011 0101
54	36	AXR		UC	6		6-9	0011 0110
55	37	SXR		EOT	7		7-9	0011 0111
56	38	LER			8		8-9	0011 1000
57	39	CER			9		1-8-9	0011 1001
58	3A	AER			:		2-8-9	0011 1010
59	3B	SER		CU3	;		3-8-9	0011 1011
60	3C	MER		DC4	<		4-8-9	0011 1100
61	3D	DER		NAK	=		5-8-9	0011 1101
62	3E	AUR			>		6-8-9	0011 1110
63	3F	SUR		SUB	?		7-8-9	0011 1111

Dec.	Hex	Instruction (RX)	Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
64	40	STH		Sp Sp	@	(3)	no punches	0100 0000
65	41	LA			A		12-0-1-9	0100 0001
66	42	STC			B		12-0-2-9	0100 0010
67	43	IC			C		12-0-3-9	0100 0011
68	44	EX			D		12-0-4-9	0100 0100
69	45	BAL			E		12-0-5-9	0100 0101
70	46	BCT			F		12-0-6-9	0100 0110
71	47	BC			G		12-0-7-9	0100 0111
72	48	LH			H		12-0-8-9	0100 1000
73	49	CH			I		12-1-8	0100 1001
74	4A	AH		¢ ¢	J		12-2-8	0100 1010
75	4B	SH	.	. .	K	8 A 8 2 1	12-3-8	0100 1011
76	4C	MH	¤)	< <	L	8 A 8 4	12-4-8	0100 1100
77	4D		[	((	M	8 A 8 4 1	12-5-8	0100 1101
78	4E	CVD	<	+ +	N	8 A 8 4 2	12-6-8	0100 1110
79	4F	CVB	¤		O	8 A 8 4 2 1	12-7-8	0100 1111
80	50	ST	& +	& &	P	8 A	12	0101 0000
81	51				Q		12-11-1-9	0101 0001
82	52				R		12-11-2-9	0101 0010
83	53				S		12-11-3-9	0101 0011
84	54	N			T		12-11-4-9	0101 0100
85	55	CL			U		12-11-5-9	0101 0101
86	56	O			V		12-11-6-9	0101 0110
87	57	X			W		12-11-7-9	0101 0111
88	58	L			X		12-11-8-9	0101 1000
89	59	C			Y		11-1-8	0101 1001
90	5A	A		! !	Z		11-2-8	0101 1010
91	5B	S	$	$ $	[	8 8 2 1	11-3-8	0101 1011
92	5C	M	*	* *	\	8 8 4	11-4-8	0101 1100
93	5D	D	]	))	]	8 8 4 1	11-5-8	0101 1101
94	5E	AL	;	; ;	¬ ^	8 8 4 2	11-6-8	0101 1110
95	5F	SL	Δ	— —	_	8 8 4 2 1	11-7-8	0101 1111
96	60	STD	-	- -	`	8	11	0110 0000
97	61		/	/ /	a	A 1	0-1	0110 0001
98	62				b		11-0-2-9	0110 0010
99	63				c		11-0-3-9	0110 0011
100	64				d		11-0-4-9	0110 0100
101	65				e		11-0-5-9	0110 0101
102	66				f		11-0-6-9	0110 0110
103	67	MXD			g		11-0-7-9	0110 0111
104	68	LD			h		11-0-8-9	0110 1000
105	69	CD			i		0-1-8	0110 1001
106	6A	AD		¦	j		12-11	0110 1010
107	6B	SD		,	k	A 8 2 1	0-3-8	0110 1011
108	6C	MD	%(	% %	l	A 8 4	0-4-8	0110 1100
109	6D	DD	¥	_ _	m	A 8 4 1	0-5-8	0110 1101
110	6E	AW	\	> >	n	A 8 4 2	0-6-8	0110 1110
111	6F	SW	¬	? ?	o	A 8 4 2 1	0-7-8	0110 1111
112	70	STE			p		12-11-0	0111 0000
113	71				q		12-11-0-1-9	0111 0001
114	72				r		12-11-0-2-9	0111 0010
115	73				s		12-11-0-3-9	0111 0011
116	74				t		12-11-0-4-9	0111 0100
117	75				u		12-11-0-5-9	0111 0101
118	76				v		12-11-0-6-9	0111 0110
119	77				w		12-11-0-7-9	0111 0111
120	78	LE			x		12-11-0-8-9	0111 1000
121	79	CE		`	y		1-8	0111 1001
122	7A	AE	¢	: :	z	A	2-8	0111 1010
123	7B	SE	# ¤	# #	{	8 2 1	3-8	0111 1011
124	7C	ME	@ '	@ @	¦	8 4	4-8	0111 1100
125	7D	DE	:	' '	}	8 4 1	5-8	0111 1101
126	7E	AU	>	= =	~	8 4 2	6-8	0111 1110
127	7F	SU	✓	" "	DEL	8 4 2 1	7-8	0111 1111

1. Two columns of EBCDIC graphics are shown. The first gives IBM standard U.S. bit pattern assignments. The second shows the T-11 and TN text printing chains (120 graphics).
2. Add C (check bit) for odd or even parity as needed, except as noted.
3. For even parity use CA.

TWO-CHARACTER BSC DATA LINK CONTROLS

Function	EBCDIC	ASCII
ACK-0	DLE,X'70'	DLE,0
ACK-1	DLE,X'61'	DLE,1
WACK	DLE,X'6B'	DLE,;
RVI	DLE,X'7C'	DLE,<

Table 2–13. Universal Code Translation (Cont.).

Dec.	Hex	Instruction and Format	Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
128	80	SSM -S					12-0-1-8	1000 0000
129	81			a	a		12-0-1	1000 0001
130	82	LPSW -S		b	b		12-0-2	1000 0010
131	83	Diagnose		c	c		12-0-3	1000 0011
132	84	WRD SI		d	d		12-0-4	1000 0100
133	85	RDD		e	e		12-0-5	1000 0101
134	86	BXH		f	f		12-0-6	1000 0110
135	87	BXLE		g	g		12-0-7	1000 0111
136	88	SRL		h	h		12-0-8	1000 1000
137	89	SLL		i	i		12-0-9	1000 1001
138	8A	SRA					12-0-2-8	1000 1010
139	8B	SLA RS					12-0-3-8	1000 1011
140	8C	SROL					12-0-4-8	1000 1100
141	8D	SLDL					12-0-5-8	1000 1101
142	8E	SRDA					12-0-6-8	1000 1110
143	8F	SLDA					12-0-7-8	1000 1111
144	90	STM					12-11-1-8	1001 0000
145	91	TM SI		j	j		12-11-1	1001 0001
146	92	MVI		k	k		12-11-2	1001 0010
147	93	TS -S		l	l		12-11-3	1001 0011
148	94	NI SI		m	m		12-11-4	1001 0100
149	95	CLI		n	n		12-11-5	1001 0101
150	96	OI		o	o		12-11-6	1001 0110
151	97	XI		p	p		12-11-7	1001 0111
152	98	LM -RS		q	q		12-11-8	1001 1000
153	99			r	r		12-11-9	1001 1001
154	9A						12-11-2-8	1001 1010
155	9B				)		12-11-3-8	1001 1011
156	9C	SIO, SIOF S			¤		12-11-4-8	1001 1100
157	9D	TIO, CLRIO S			'		12-11-5-8	1001 1101
158	9E	HIO, HDV S			±		12-11-6-8	1001 1110
159	9F	TCH S			≡		12-11-7-8	1001 1111
160	A0				~		11-0-1-8	1010 0000
161	A1			~	^		11-0-1	1010 0001
162	A2			s	s		11-0-2	1010 0010
163	A3			t	t		11-0-3	1010 0011
164	A4			u	u		11-0-4	1010 0100
165	A5			v	v		11-0-5	1010 0101
166	A6			w	w		11-0-6	1010 0110
167	A7			x	x		11-0-7	1010 0111
168	A8			y	y		11-0-8	1010 1000
169	A9			z	z		11-0-9	1010 1001
170	AA						11-0-2-8	1010 1010
171	AB				↳		11-0-3-8	1010 1011
172	AC	STNSM SI			¬		11-0-4-8	1010 1100
173	AD	STOSM SI			[		11-0-5-8	1010 1101
174	AE	SIGP -RS			≥		11-0-6-8	1010 1110
175	AF	MC -SI			◆		11-0-7-8	1010 1111
176	B0				0		12-11-0-1-8	1011 0000
177	B1	LRA -RX			1		12-11-0-1	1011 0001
178	B2	See below			2		12-11-0-2	1011 0010
179	B3				3		12-11-0-3	1011 0011
180	B4				4		12-11-0-4	1011 0100
181	B5				5		12-11-0-5	1011 0101
182	B6	STCTL RS			6		12-11-0-6	1011 0110
183	B7	LCTL			7		12-11-0-7	1011 0111
184	B8				8		12-11-0-8	1011 1000
185	B9				9		12-11-0-9	1011 1001
186	BA	CS RS					12-11-0-2-8	1011 1010
187	BB	CDS			↵		12-11-0-3-8	1011 1011
188	BC				↑		12-11-0-4-8	1011 1100
189	BD	CLM			]		12-11-0-5-8	1011 1101
190	BE	STCM RS			←		12-11-0-6-8	1011 1110
191	BF	ICM			←		12-11-0-7-8	1011 1111

Dec.	Hex	Instruction (SS)	Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
192	C0		?	{		8 A 8 2	12-0	1100 0000
193	C1		A	A	A	8 A 1	12-1	1100 0001
194	C2		B	B	B	8 A 2	12-2	1100 0010
195	C3		C	C	C	8 A 2 1	12-3	1100 0011
196	C4		D	D	D	8 A 4	12-4	1100 0100
197	C5		E	E	E	8 A 4 1	12-5	1100 0101
198	C6		F	F	F	8 A 4 2	12-6	1100 0110
199	C7		G	G	G	8 A 4 2 1	12-7	1100 0111
200	C8		H	H	H	8 A 8	12-8	1100 1000
201	C9		I	I	I	8 A 8 1	12-9	1100 1001
202	CA						12-0-2-8-9	1100 1010
203	CB						12-0-3-8-9	1100 1011
204	CC			<			12-0-4-8-9	1100 1100
205	CD						12-0-5-8-9	1100 1101
206	CE			+			12-0-6-8-9	1100 1110
207	CF						12-0-7-8-9	1100 1111
208	D0		!	}		8 8 2	11-0	1101 0000
209	D1	MVN	J	J	J	8 1	11-1	1101 0001
210	D2	MVC	K	K	K	8 2	11-2	1101 0010
211	D3	MVZ	L	L	L	8 2 1	11-3	1101 0011
212	D4	NC	M	M	M	8 4	11-4	1101 0100
213	D5	CLC	N	N	N	8 4 1	11-5	1101 0101
214	D6	OC	O	O	O	8 4 2	11-6	1101 0110
215	D7	XC	P	P	P	8 4 2 1	11-7	1101 0111
216	D8		Q	Q	Q	8 8	11-8	1101 1000
217	D9		R	R	R	8 8 1	11-9	1101 1001
218	DA						12-11-2-8-9	1101 1010
219	DB						12-11-3-8-9	1101 1011
220	DC	TR					12-11-4-8-9	1101 1100
221	DD	TRT					12-11-5-8-9	1101 1101
222	DE	ED					12-11-6-8-9	1101 1110
223	DF	EDMK					12-11-7-8-9	1101 1111
224	E0			\		A 8 2	0-2-8	1110 0000
225	E1						11-0-1-9	1110 0001
226	E2		S	S	S	A 2	0-2	1110 0010
227	E3		T	T	T	A 2 1	0-3	1110 0011
228	E4		U	U	U	A 4	0-4	1110 0100
229	E5		V	V	V	A 4 1	0-5	1110 0101
230	E6		W	W	W	A 4 2	0-6	1110 0110
231	E7		X	X	X	A 4 2 1	0-7	1110 0111
232	E8		Y	Y	Y	A 8	0-8	1110 1000
233	E9		Z	Z	Z	A 8 1	0-9	1110 1001
234	EA						11-0-2-8-9	1110 1010
235	EB						11-0-3-8-9	1110 1011
236	EC			<			11-0-4-8-9	1110 1100
237	ED						11-0-5-8-9	1110 1101
238	EE						11-0-6-8-9	1110 1110
239	EF						11-0-7-8-9	1110 1111
240	F0	SRP	0	0	0	8 2	0	1111 0000
241	F1	MVO	1	1	1	1	1	1111 0001
242	F2	PACK	2	2	2	2	2	1111 0010
243	F3	UNPK	3	3	3	2 1	3	1111 0011
244	F4		4	4	4	4	4	1111 0100
245	F5		5	5	5	4 1	5	1111 0101
246	F6		6	6	6	4 2	6	1111 0110
247	F7		7	7	7	4 2 1	7	1111 0111
248	F8	ZAP	8	8	8	8	8	1111 1000
249	F9	CP	9	9	9	8 1	9	1111 1001
250	FA	AP		!			12-11-0-2-8-9	1111 1010
251	FB	SP					12-11-0-3-8-9	1111 1011
252	FC	MP					12-11-0-4-8-9	1111 1100
253	FD	DP					12-11-0-5-8-9	1111 1101
254	FE						12-11-0-6-8-9	1111 1110
255	FF			EO			12-11-0-7-8-9	1111 1111

One example is identified below:

Step 1: Write the pattern desired bit by bit in the following format with the first transmitted bit first. An example T1 CSU Loop Up set code pattern is shown below (a continual repeating 10000).

1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 ———

Step 2: Table 2–6 is constructed so that the least significant bit (LSB) is the inverse of what normally would be expected. This is a reference to allow the user to easily "invert" the desired pattern.

Step 3: Segment the pattern into 8–bit bytes as shown below until the pattern repeats. In this example the pattern repeats after the fortieth bit.

10000100 00100001 00001000 01000010 00010000 10000100

Step 4: Compare the first byte (10000100) to the various bytes in Table 2–6 and note that it is identical to the pattern for the HEX character set "21".

Step 5: Compare the second byte (00100001) to the tabulated values and note that it is equivalent to HEX "84".

Step 6: Repeat the procedure for all the remaining bytes. The 40–bit long pattern equates to the HEX character string "21 84 10 42 08"

Step 7: The repetitive 10000 pattern has thus been converted into its HEX pattern "21 84 10 42 08" into the USER PATTERN display and the pattern generated will be a continuous 1000010000 . . .

NOTE This sample pattern (10000) is the Set Code used to loop back a T–1 Channel Service Unit (CSU) such as the Phoenix Model 1544.

An example of another use is a pattern with a long string of 0's to stress test a regenerative repeater's clock recovery and reshaping capability. Let us assume that the user desires a string of 31 0's. It is necessary to have at least one "1" in the string so the pattern would look like:

10000000 00000000 00000000 00000000 100... etc.

HEX 1 HEX 0 HEX 0 HEX 0

The user would enter the pattern in HEX as "01 00". This would be a 31 zero transmission followed by a 1 and another string of 31 zeroes and so on. With practice the user can input almost any binary pattern desired. The only restriction is that the pattern must be able to repeat within 2048 bytes.

2.4.12 BIG BERT Display

The BIG BERT Display is provided as a convenience for the user. This menu allows the selection and display of any two of the error measurement parameters which are accumulated by the 5500A. The BIG BERT Display is a split screen, large format display as shown in Figure 2–19. The user may choose a parameter for display by using the UP/DOWN CURSOR keys to place the half intensity block in the top or bottom half of the display. Then, using the select keys, the user may scroll through any of the parameters being measured and display whichever one is desired. This does not interfere with the test in progress.

2.4.13 Digital Data Trap Menu

The 5500A has a digital data trap which permits the user to monitor a digital data line and 'trap' 64K bits of data in a buffer for examination on a bit–by–bit basis. In addition, 17599 bits (2200 bytes) of the trapped data can be placed into the 5500A's user pattern (User Pattern #4) to be used to recreate the exact pattern that has caused the bit error (the digital data trap only triggers on bit errors and must be in pattern sync; however, future software releases may expand the trigger selection to include other error events). The data is trapped relative to the position of the trigger as

Figure 2–19. Big BERT Display.

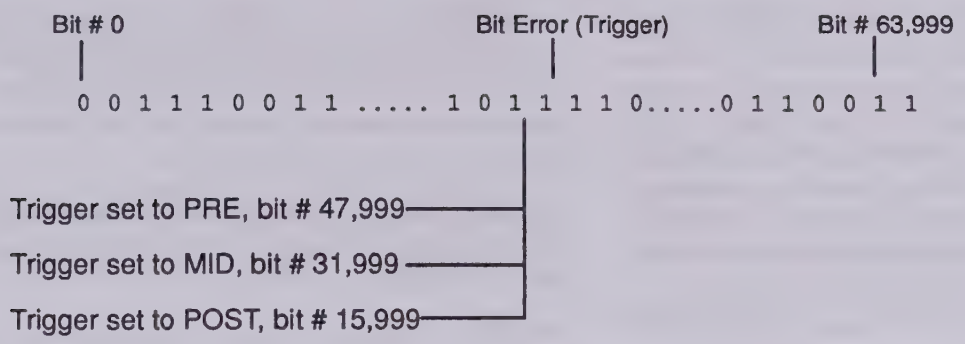

Bit # 0
Bit Error (Trigger)
Bit # 63,999
0 0 1 1 1 0 0 1 1 ..... 1 0 1 1 1 1 0.....0 1 1 0 0 1 1
Trigger set to PRE, bit # 47,999
Trigger set to MID, bit # 31,999
Trigger set to POST, bit # 15,999

Figure 2–20. Bit Relationship in Data Trap Buffer.

shown in Figure 2–20. When PRE is selected, the trigger is positioned with 48K bits of pre data and 16K bits of post data. When MID is selected, there are 32K bits on either side of the trigger. When POST is selected, the trigger is positioned with 16K bits of pre data and 48K bits of post data.

The Digital Data Trap Menu, shown in Figure 2–21, is used to display the bit–by–bit history of a trapped event. The softkeys associated with this menu are the START and STOP keys, which start and stop the trap mode, and the USER/CAN key, which is used to move the selected portion of the data that has been trapped into user pattern #4.

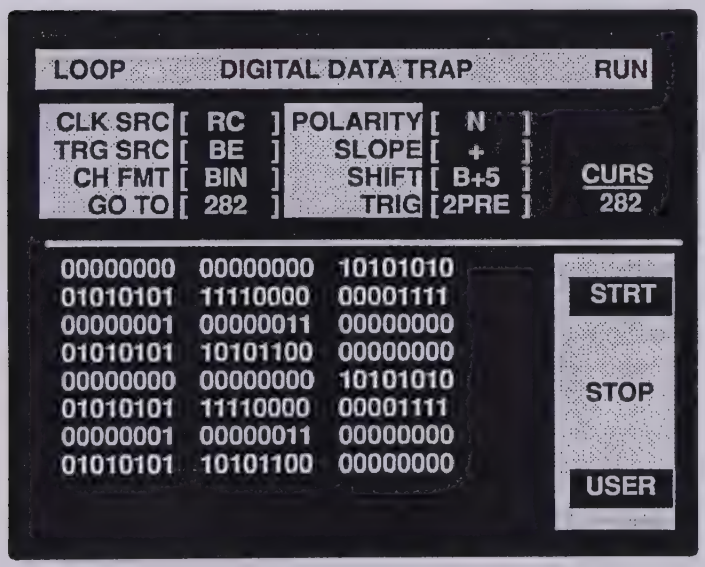


Figure 2–21. Digital Data Trap Display.

NOTE Obviously, any pattern could be trapped and placed into the user pattern for testing. This may result in a pattern that does not fall within the pattern sync criteria of the 5500A. If that is the case, the 5500A will **NOT** obtain pattern sync. However, the pattern may still be used for testing the network for problems other than pattern sync problems.

To use the data trap and user pattern feature, after the 5500A is connected to the circuit to be tested, follow the steps below:

1. Move the cursor to the TRIG field and set the data trap trigger to the desired location relative to the bit error. The 5500A utilizes three triggers; PRE, MID, and POST. When PRE is selected, the trigger is positioned with 48K bits of pre data and 16K bits of post data. When MID is selected, there are 32K bits on either side of the trigger. When POST is selected, the trigger is positioned with 16K bits of pre data and 48K bits of post data.
2. Move the cursor to the CH FMT field and select the desired format for viewing the trapped data. This field may be changed at any time after the data has been trapped and will change the format of the data displayed, but not the data. Refer to the paragraphs below for additional information on display format
3. Press the **STRT** softkey to arm the trap.
4. After the data trap has "triggered" (indicated by the display filling with data) and a segment of data has been trapped, press the **USER** softkey if you wish to place a portion of the trapped data into user pattern #4.

3. The Bit Trap Menu will change and appear as shown in Figure 2–22.
4. Select the bit within the trapped data at which you wish the user pattern to begin. Move the cursor over the BEGIN field and enter the number of the beginning bit in the BEGIN field (if you do not know the number of the desired bit, you can determine the number by placing the cursor over the desired bit and reading the number of the bit under the CURS field on the display).

CAUTION Whenever user pattern 4 is selected, the data in that location will be overwritten and lost when the "trapped" pattern is entered.

---

6. Determine the desired length of the pattern you wish to place in user pattern #4 and enter that length (in bits) in the LNGH field (the maximum length is 17599).

CAUTION Pressing the CAN softkey at any time while in this menu, will cancel all operations and return you to the main Bit Trap Menu without storing a pattern in the user pattern memory.

---

7. Press the STOR softkey. This transfers the "trapped" pattern to user pattern #4.

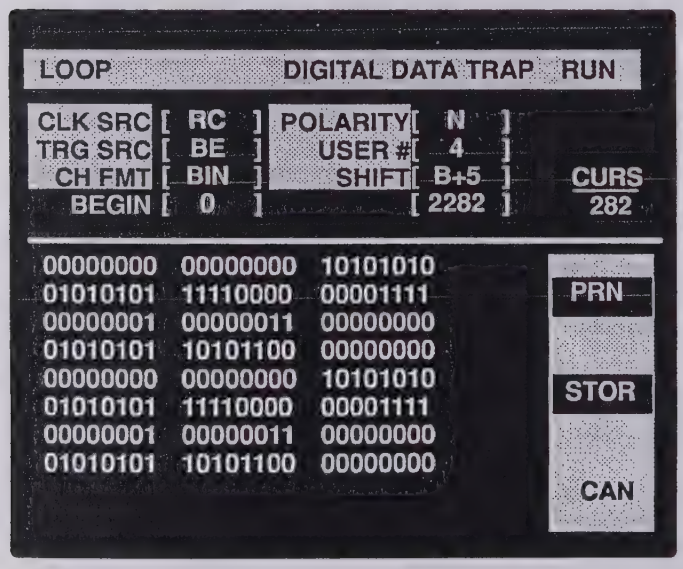


Figure 2–22. Digital Data Trap Display After User Softkey is Pressed.

8. Verification of the pattern transfer may be accomplished by selecting USER PATTERN Menu and viewing the pattern stored in user pattern #4.

The remaining lines on the main Bit Trap Menu are as follows:

CLK SRC – The clock source is the receive clock. Future software enhancements may permit user selection of other clock sources.

TRG SRC – The trigger source is bit errors (BE). Future software enhancements may permit user selection of other trigger sources.

GO TO – A number may be entered here from the front panel keyboard to place the cursor anywhere within the 64,000 bit buffer. The number may be any number between 0 and 63,999. The value entered will flash until the 'E' (**ENTER**) key is pressed to validate setting.

C "CLEAR" – This key on the keypad is used to clear the GO TO, BEGIN, and LNGH fields.

POLARITY – The polarity is a default setting to obtain optimum performance. The polarity line is on the menu to permit future software enhancements which may permit user selection of the trigger polarity.

SLOPE – The slope is a default setting to obtain optimum performance. The slope line is on the menu to permit future software enhancements which may permit user selection of the trigger slope.

SHIFT – The user may shift the data bits being viewed on the screen from –7 to +7 bits. This also changes the LSB and MSB of the eight–bit bytes and will change the HEX value of the bytes.

CH FMT – The user may view the data stored in the trap in either binary (BIN) or hexidecimal in (HXL [LSB] or HXM [MSB]).

The Digital Data Trap Menu displays binary received data in the order that it was received relative to time, left–to–right, top–to–bottom, on the screen. The binary bit in the upper left corner was received first and the binary bit in the lower right corner was received last (the bit highlighted is the bit on which the bit trap triggered). The binary data is organized on 8–bit boundaries to facilitate conversion to HEX data. The data may be shifted left or right 8 bits in either direction to group any consecutive 8 bits into 8–bit words. Since the binary data is displayed in the order it was received (left–to–right, top–to–bottom) the

leftmost bit in each 8–bit boundary was received **first**, followed by the 7 bits immediately to its right. To convert the binary data to HEX data, the user must select either HXL or HXM format in the CH FMT field on the display. HXL format defines the leftmost bit (first received) of each 8–bit word as the LSB (least significant bit) and creates a "LSB FIRST RECEIVED" HEX word. HXM format defines the leftmost bit of each 8–bit word as the MSB (most significant bit) and creates a "MSB FIRST RECEIVED" HEX word.

For example:

8–bit Binary word received as displayed:

First Bit Received

0 0 0 0 1 0 1 0

Converts to HXL hex word = 50 LSB 1st

Converts to HXM hex word = 0A MSB 1st

To illustrate this point, take the case of the 5500A USER PATTERN. Data is entered into the user pattern in HEX format. When a HEX word is written as binary, the MSB is normally on the left and the LSB is normally on the right.

For example:

50 hex

0 1 0 1 0 0 0 0 binary

MSB LSB

When a user pattern HEX word is transmitted, it is transmitted LSB FIRST. That is, the first bit transmitted of the HEX word 50 would be a "0" followed by "0–0–0–1–0–1" followed by the MSB "0" transmitted last. When this byte is received and displayed in binary format by the Digital Data Trap, it would appear as:

0 0 0 0 1 0 1 0

because the first bit received is always displayed as the leftmost bit in each 8–bit word. The digital trap has no way of knowing whether the binary data it received arrived LSB FIRST or MSB FIRST. The trap only displays binary data in the order that it was received relative to time (left–to–right, top–to–bottom). It is up to the user to determine whether the MSB or the LSB of an 8–bit byte was received first. In the above example, the LSB was received first. Therefore the user would select the HXL format to convert the binary data to HEX, and display the received user pattern.

2.4.14 Miscellaneous Menus

The optional displays (High Speed Jitter, MSU Configuration, etc.) are discussed in the applicable option manual. The G.821 performance monitoring menu is discussed in section 6, Performance Monitoring.

2.5 FREQUENCY MEASUREMENT

The 5500A is also a frequency counter with a resolution of 0.1 Hz below 1 MHz and 1 Hz above 1 MHz. The reading is displayed on the BERT RESULTS Menu as shown in Figure 2–10. The user may select BR to view the asynchronous Baud Rate, or TC (Transmit Clock), RC (Receive Clock) or XC (External Clock) in synchronous system testing.

The 5500A counter provides the user with a reasonably accurate diagnostic tool for uncovering frequency related error problems. This enables the user to spot a drifting clock. When the test set is set up in the EXT clock mode, the user can measure and determine the stability of the receive clock by selecting RC. When acting as a synchronous DTE it is convenient to check the outgoing clock by selecting TC. The user can easily compare the transmit and receive clocks for significant differences. When a USER clock input to the rear panel BNC connector has been selected, the user can measure it on the TC of transmit clock field.

The user may measure the external clock (Pin 24 on the RS–232 interface module) signal by selecting XC. This would be used when the 5500A is deriving its clock from an external source such as a modem or terminal to time its transmitter.

Frequency counter display accuracy is a function of the internal 4.608 MHz reference clock oscillator. The 5500A uses a software controlled correction to "zero out" the impact of the crystals in accuracy. All that remains is the effect of thermal stability or drift. This is typically less than 2–1/2 parts per million with the standard crystal.

2.6 TIME MEASUREMENTS

2.6.1 Event Timing

The 5500A measures the time interval between transitions of any two selected interface signals (listed below) to 4.67

minutes duration with a resolution of 1 microsecond to 10 milliseconds depending upon scale.

RTS /	DTR /
RTS \	DTR \
RD /	DCD /
RD \	DCD \
TD	DSR /
TD \	DSR \
SQ /	CTS \
SQ /	CTS \

The "/" character after a signal indicates that signal going "TRUE". For an RS–232 interface, a MARK to SPACE (1 to 0) transition is the TRUE condition. The "\" character shows a transition to FALSE. On a TTL interface a "HIGH" to "LOW" transition is the TRUE condition. If an "I" is displayed, valid transitions have occurred, and an "I" for indeterminate is shown.

The user selects the resolution as 1us, 10us, 100us, 1MS, or 10MS, and then chooses which two events are to be measured. The 5500A automatically measures the time delay between the transitions, and updates the measurements display on a continuous basis.

2.6.2 Network Loop Timing

The 5500A is equipped with a network loop delay timer. The timer can operate while any of the pseudorandom patterns are being generated by the 5500A and looped back to the 5500A from some point in the network. An example is presented in Figure 2–23.

In the example shown, the 5500A is transmitting through 2 switches to a DTE. The DTE is set to loop the signal back

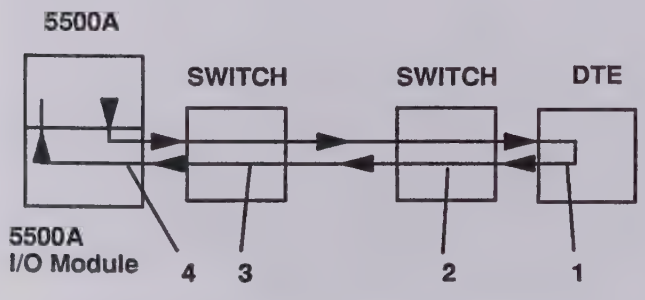


Figure 2–23. 5500A Network Loop Delay.

(point 1) along the path to its source. In this configuration the 5500A will measure the total loop time for the entire path.

In the event the user desires to measure only parts of the path, a tare function is included with the timer circuit. Any section of the path that can be set to loop back can be subtracted from the total loop time. This subtracted time is referred to as the tare value. If, for example, a loop back was placed at position 4, the loop delay timer can be set to tare the delay in the 5500A I/O module. Then when the configuration is returned to loop back at position 1, the delay inherent in the I/O module will be subtracted and the loop time which is displayed is the delay time contained in all of the network external to the 5500A.

In a similar manner, tare values could be established by looping the network at points 2 or 3 to pin–point a delay to a particular circuit/component.

The network loop delay timer can measure times to 17 minutes and can display loop times in the following ranges of resolution; 1 usec, 10 usec, .1 Msec, 1 Msec, 10 Msec.

2.7 BIAS DISTORTION (SKEW)

The 5500A measures BIAS DISTORTION on the receive data lines. A pattern having a uniform 50/50 distribution of 1's and 0's is customarily used as the transmitted signal. Any of the 5500A pseudorandom sequences may be used.

Bias is determined as a ratio of MARKS (1's) to SPACES (0's) and expressed as a percentage.

A reading of 0% indicates a constant SPACE signal while a reading of 100% indicates a constant MARK signal. A 50% reading indicates ideal symmetry of MARK bit widths periods to SPACE bit widths periods.

A reading of 45% to 55% is considered acceptable in most systems. Some older modems may have larger windows of acceptable performance but in general readings outside the 45–55% range may be cause for further investigation.

If a modem or other device has filters shaping the bit stream, and they have degraded band pass characteristics which favor 1's over 0's or vice versa, then the likelihood of an error occurring is increased.

Bias Distortion was more of a problem with older FSK type modems employing lumped element filters than it is with modern modems which use digital filter techniques.

Bias Distortion measurement accuracy is +1%, and the reading is updated at least once per second.

2.8 BER TEST TROUBLESHOOTING

Table 2–14 presents a list of possible problem areas and possible solutions if the 5500A does not achieve synchronization with the device under test.

2.9 ACTIVITY INDICATORS

There are 12 green LED's on the 5500A front panel to indicate activity of the installed interface module.

The actual points being monitored are on the TTL interface between the module and control board. Since there are many different module options, all front panel indicators may not be applicable to a particular interface.

In addition, some of the indicators change meaning when modes are switched between DTE and DCE.

Table 2–15 and Table 2–16 relate the LED's to the interface circuit being monitored, for each module and mode of operation.

The LED indicators provide interface activity status as well as mode (RUN), async, sync recovery, and error injection status. For example, if the 5500A is transmitting data and the TD LED is lit, but there is no received data (RD LED not lit), then it is possible that the transmission source at the distant end is not functioning. This could be a modem which is receiving data but whose transmit section has become defective.

Table 2–14. BER Test Troubleshooting.

PROBLEM	CORRECTIVE ACTION
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Check bit rates, sync/async mode, character size, parity, etc. Verify correct mode (DCE or DTE) has been selected. Verify correct mode (RTS/DCD) has been selected. Verify BRIDGE mode in T–Carrier testing has not been selected. (BRIDGE mode disables the 5500A transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify item under test is not open circuited.
Continuous Bit Error Indicated	If two 5500A test sets are connected for end–to–end testing, make sure the bit rates, patterns, modes, etc. are the same in both units. Also, in SYNC mode, ensure that one unit supplies clock and the other is set to EXT clock.
SYNC LED blinks on and off in synchronous testing	If two test sets are operating in an end–to–end test, verify that one is set to supply clock (internal timing) and the other is set to EXTERNAL clock. If a modem or other device in the circuit is the master clock, set both sets to EXTERNAL. Note: There can be only one Master Clock in a synchronous circuit.
SYNC LED not illuminated and TD LED is off	Verify RTS is activated if unit is configured as DTE.
Constant bursts of errors detected in testing synchronous devices	Select External clock mode if not already selected. (Most synchronous devices are strapped to supply clock).
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.

Table 2–14. BER Test Troubleshooting.(Cont.).

PROBLEM	CORRECTIVE ACTION
Test suddenly stops and RUN LED goes off.	If continuous testing is desired, verify that "00:00:00" (or for BLOCKS set to 0) has been placed in the test time window and press RUN. If testing for a specific time, verify that the time selected has elapsed when set stops. This is normal operation.
5500A displays errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. Note that T1 carrier systems are only specified to provide a 1x10–6 error/bit rate which is about three errors or less every two seconds.
RAM error on power–up	Battery may be discharged. Power test set for 24 hours to charge up battery.

Table 2–15. RS–232/RS–449 Activity Indicators.

INDICATOR	ACTIVITY			
	RS–232		RS–449	
	DTE	DCE	DTE	DCE
TD/RD	Xmit Data	Rx Data	Send Data	Receive Data
RD/TD	Rx Data	Xmit Data	Receive Data	Send Data
RC/RC	Rx Clock	Rx Clock	Receive Timing	Receive Timing
TC/TC	Tx Clock	Tx Clock	Xmit Timing	Xmit Timing
RTS/DCD	Request to Send	5500A Data Carrier Det.	Request to Send	Receive Ready
CTS/RTS	Clear to Send	Clear to Send	Clear to Send	Request to Send
DSR/DTR	DSR	DTR	Data Mode	Terminal Ready
DTR/DSR	DTR	DSR	Terminal Ready	Data Mode
DCD/CTS	Data Carrier Det	Clear to Send	Receiver Ready	Clear to Send
RI/RI	Ring Indicator	Ring Indicator	Incoming Call	Incoming Call
SQ/SQ	Signal Quality	Signal Quality	Signal Quality	Signal Quality
SCTE/SCTE	SCTE	SCTE	Terminal Tim	Terminal Tim

Table 2–16. T1/T1C and V.35 Activity Indicators.

INDICATOR	ACTIVITY			
			V.35	
	T1/T1C	Framed T1	DTE	DCE
TD/RD	Xmit Data	Xmit Data	Xmit Data	Receive Data
RD/TD	Receive Data	Receive Data	Receive Data	Xmit Data
RC/RC	Recovered Rec Clock	Gated Internal Clock	Element Timing Xmit Signal	Element Timing Xmit Signal
TC/TC	Recovered Xmit Clock	Gated Internal Clock	Element Timing	Element Timing Data Chann Rec
RTS/DCD	X*	X*	Request to Send	Line Signal Det
CTS/RTS	X	N/A	Ready for Send	Request to Send
DSR/DTR	X	X	Data Set Ready	Data Terminal Ready
DTR/DSR	X*	X	Data Terminal Ready	Data Set ready
DCD/CTS	X	X*	Receive Data Channel Receive Line Signal Detector	Drive ready for Sending
RI/RI	X	X	Calling Indicator	Calling Indicator
SQ/SQ	X	X	X X	
SCTE/SCTE	Internal Clock Source	Gated Recovery Receive Clock	Transmitter Signal Element Timing (DTE Source)	Transmitter Signal Element Timing (DTE Source)

* May be control signals pertinent to internal 5500A functions on these monitored lines.

2.10 PROGRAMMABLE USER PATTERN

T1 facilities are increasingly being used to transport high speed data between computers and workstations as well as for video conference applications. This has brought about the development of products for the conversion of V.35 and RS–449 data interfaces into a format compatible with the T1 network. One such product is the TXPORT 1536 Data T. In simplest form this product converts the 1.544Mbps clock and data of the DTE into the bipolar format required by the T1 network. On the receive side it performs the reverse operation converting the bipolar data back into data and clock. Depending upon the network, the T1 side may require framing and the DTE may take on this responsibility. However, turn up or maintenance testing of a network configured in this manner can be problematic because of the need to generate V.35 or RS–449 patterns which contain T1 framing.

Following is one example of how this can be accomplished with the 5500A's programmable user pattern.

The pattern to be generated consists of the ASCII encoded phrase "Phoenix D4 Frame Test XX". "XX" represents an incrementing two–digit number which ranges from 00 in the first frame to 23 in the last frame of the pattern. The length of the test phrase was chosen to be 24 characters to match the 24 channels in a T1 frame. The first frame is modified to start with a unique 3–byte sync pattern having the HEX values of FF AA AA. The remainder of the first frame is "Phoenix Sync Frame 00". The total number of frames was chosen such that the D4 frame pattern would repeat and the total pattern length would be a multiple of eight bits as required by the 5500A. The resulting user pattern is 579 bytes long. Notice that the first three bytes of the user pattern are the unique sync pattern. The pattern has been organized so that the three bytes can be easily modified without affecting the D4 frame bits.

An accompanying basic program is provided in Table 2–17 which generates this pattern with additional formatting which will allow it to be sent to the 5500A's remote port to directly program user pattern 4. This program could be modified to change the data content of the frames, to provide ESF framing, or for other reasons.

Table 2–17. 5500A Programmable User Pattern

```
REM
REM This routine generates an ASCII text file which when
sent to the 5500A's remote port configures USER Pattern 4
to a 2 super frame lang, D4 framed test sequence.
    WIDTH 66
REM Open destination file
    OPEN "o" ,1, " fh1:testpattern "
REM Define some constants
    ff$ = CHR$(&HFF):                    REM define HEX "FF"
    aa$ = CHR$(&HAA):                    REM define HEX "AA"
    ffs$ = ff$ + aa$ + aa$:              REM define unique 3 byte sync pattern
    frame1$ =ffs$+"Phoenix Sync Frame 00": REM Frame 1 Data
    framenS = "Phoenix D4 Frame Test ":  REM Constant Data for remaining Frames
REM Build string with text for frames 1 to 23
    FOR n=1 T0 23
        framex$ = framex$ + framen$ +
        RIGHT$(STR$(100+n),2)
    NEXT n
REM Full text string is frame 00 + frames 1 to 23
    framedata$ = frame1$ + framex$
REM The following data statements hold the D4 frame bit
sequence. Note: the pattern is stored starting at the 2nd bit
in the sequence and two full super frames are presented.
```

Table 2–17. 5500A Programmable User Pattern (Cont.).

```
    DATA 0,0,0,1,1,0,1,1,1,0,0,1
    DATA 0,0,0,1,1,0,1,1,1,0,0,1
REM Setup various indexes
    n= 0 :                          REM Bit position index for extracting bits from the
                                    frame data string
    m = 0 :                         REM Bit position index for assembling bits into the
                                    output file
    i = 1 :                         REM Position index for extracting data from the frame
                                    data string

REM Generate the user pattern by combining the data text
with the frame  bits and output to the file with the appropri-
ate 5500A commands for setting user pattern 4.
    PRINT #1,"USRPAT = 4":          REM 5500A command to select user pattern 4
    lead$ = "USRPAT" :              REM Initialize lead string with 5500A command to set
                                    user pattern data
    FOR g  = 1 TO 24:               REM Total of 24 frames
        GOSUB doframe:              REM Generate data for 1 frame
        READ bit:                   REM Read frame bit state from data statement
        GOSUB outchars:             REM Add frame bit to pattern
    NEXT g:                         REM Loop until all 24 frames are output
    CLOSE:                          REM Close output file
    STOP:                           REM That's all
REM What follows are subroutines called from above
REM The following subroutine reads 192 bits from the data
string and formats them for output.
doframe:
    fbit = 1:                       REM Initialize bits in frame counter
loop:
REM Is it time to get next character from frame DATA  string
    IF n = 0 THEN
        word = ASC (MID$ (framedata$, i, 1 ) ) :   REM Yes, get one character
        i = i+1:                    REM Advance index
    END IF
    GOSUB getnextmask:              REM Get mask to disassemble frame data
                                    into bits

REM Set "bit" from frame data
    IF ((word AND mask) <> 0) THEN
        bit = 1
        ELSE
        bit = 0
    END IF
```

Table 2–17. 5500A Programmable User Pattern (Cont.).

```
    GOSUB outchars:                          REM Add "bit" to output Pattern
    fbit = fbit + 1:                         REM Advance count of bits in frame
    IF fbit < 193 GOTO loop:                 REM Loop until 192 data bits have been output
RETURN:                                      REM 192 bits have been moved from frame data
                                             string to output. Its time for a frame bit now.

REM This subroutine generates the next mask for extracting
bit data from the frame data string.
getnextmask:
    mask = 2^n:                              REM mask is 1, 2, 4
     n = (n+1) MOD 8:                        REM advance mask index
RETURN
REM This subroutine assembles bits into the output file
outchars:
    masko = 2^m:                             REM Output bits position
    m = (m+1) MOD 8:                         REM Advance mask index
    byte = bit * masko + byte:               REM Build output byte from previous bits + this
REM Has a full bytes been assembled
    IF m = 0 THEN
REM Yes, is this start of a LINE
    IF chars = 0 THEN
        PRINT #1,1ead$;:                     REM Yes, output 5500A command
        lead$ = "USRPAT +":                  REM Update 5500A command to append remaining
                                             lines
    END IF
    PRINT #1, " " ;RIGHT$( "0"+HEX$(byte),   REM add byte to output file
    2);:
    byte = 0:                                REM Initialize to start assembly of next byte
    chars = chars + 1:                       REM Advance characters on line counter
REM Is it time to start a new line?
    IF chars = 9 THEN
        PRINT #1, " "                        REM Yes, terminate this line
        chars = 0:                           REM Initialize characters counter
        END IF
    END IF
RETURN
```

2.11 MOUNTING

2.11.1 Bench Top

The 5500A, as shipped from the factory, is designed to be used on a flat work surface. The front feet are designed to be used in two positions; 1) folded back, the 5500A is in a level position, and 2) when folded down, the front of the 5500A is raised approximately 3 inches, providing a better viewing angle when the 5500A work surface is at standard table height.

2.11.2 Standard Rack Mount

The 5500A–RK–19 rack mount kit allows the user to mount the 5500A into a standard 19–inch rack.

The rack mount kit includes two (2) interchangeable Rack Mount Ears and ten (10) #8–32 Phillips screws. A Phillips screwdriver is also required which is not included in this kit. Proceed as follows to rack mount the 5500A.

1. Locate the five holes on each side of the test set.
2. Remove the two screws and handle on each side of the test set.
3. Remove the four feet on the bottom panel of the test set.
4. Remove the four feet on the right side panel of the test set.
5. Align the holes in one rack mount ear with the five holes on one side of the test set.
6. Assemble rack mount ears to main chassis using five #8–32 screws.
7. Repeat this procedure for the opposite side of the chassis.

2.12 PRE–INSTALLATION CHECK

The 5500A may be operated from any power source supplying 100 to 130 Vac, 220 to 240 Vac, 47 to 66 Hz, single phase.

In some applications, if the ac power has high voltage spikes, it may be necessary to add a ground wire from the chassis ground lug on the rear panel to facility (earth) ground.

WARNING Damage to the unit may result if the line voltage is not selected to match the input power source.

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Chapter 3 – Operation

3.0 INTRODUCTION

This section of the manual provides operation procedures for the most commonly used tests using the 5500A test set. Procedures include an initial power up procedure and procedures for an out–of–service bit error rate test, clock/frame slip, in–service drop/insert, in–service monitoring, and a DCE BERT test.

The following instructions are written with the assumption that the user is familiar with the 5500A test set. For an overview of test set operation, refer to section 2.

3.1 INITIAL POWER UP AND MENU SETUP

The following instructions are general power up and menu setup procedures. These instructions may be followed for all interface modules.

1. With power removed, plug the desired interface module into the rear panel slot on the 5500A and secure with the two retaining screws.

2. Turn the power switch to on and verify the display is activated. Adjust the intensity if the CRT is dim.

3. The first item to appear will be either the BERT SETUP Menu (Figure 3–1) or the 5500A CONFIGURATION display (Figure 3–2). The BERT SETUP Menu appears to indicate the test set has passed the self test and is ready for setup and testing.

4. If the 5500A CONFIGURATION Menu is displayed, the 5500A has failed the self–test, the Ni–Cad battery may be discharged or dislodged, or the USER PROGRAM or USER PATTERN has an error or has not been programmed. If the display indicates a ROM or RAM failure, return to step one and begin this procedure again. If the problem persists, the test set is in need of maintenance. If the USER PROGRAM or USER PATTERN indicates invalid, do not use the stored pattern/program until it has been verified that the failure is due to battery failure. To change the INVALID indication, complete the following steps for USER PATTERN or USER PROGRAM INVALID indications.

   USER PATTERN

   a. At the USER PATTERN Menu, verify the user pattern 1 through 4 does not contain an error. If the pattern does contain an error, position the cursor to the errored byte and use the HEX keypad to enter the correction.

   b. Another alternative to clear the INVALID indication is to clear the each entire user pattern. By enabling the CLR softkey twice on the USER PATTERN Menu the entire user pattern will be cleared from memory.

   c. Proceed to the CONFIGURATION Menu and verify the USER PATTERN reads PASS.

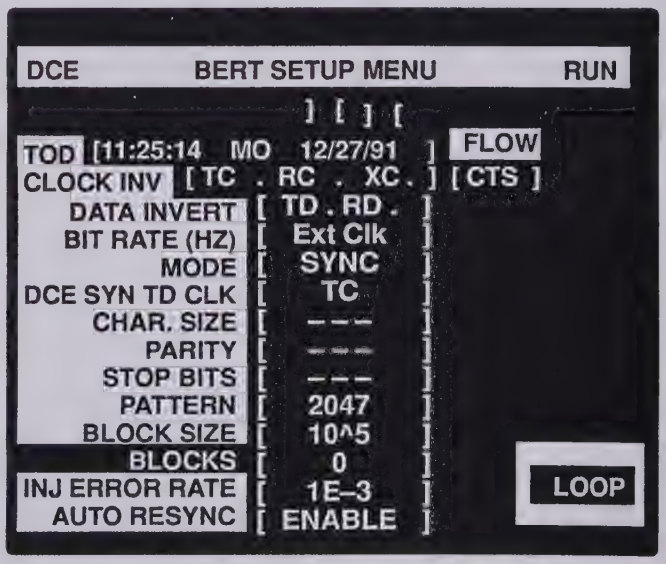
DCE
BERT SETUP MENU
RUN
TOD [11:25:14 MO 12/27/91]
FLOW
CLOCK INV [TC . RC . XC .] [CTS]
DATA INVERT [TD . RD .]
BIT RATE (HZ) [Ext Clk]
MODE [SYNC]
DCE SYN TD CLK [TC]
CHAR. SIZE [---]
PARITY [---]
STOP BITS [---]
PATTERN [2047]
BLOCK SIZE [10^5]
BLOCKS [0]
INJ ERROR RATE [1E–3]
AUTO RESYNC [ENABLE]
LOOP

Figure 3–1. RS–232 BERT SETUP Menu.

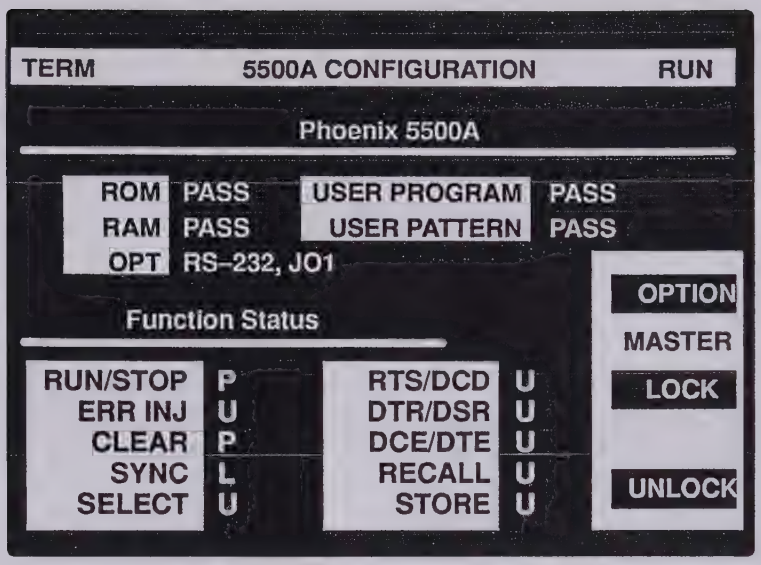

Figure 3–2. 5500A CONFIGURATION Display.

USER PROGRAM

a. Turn power off and back on.

b. Verify the CONFIGURATION MENU USER PROGRAM reads PASS. If INVALID indication is still present, all user programs must be cleared.

c. Proceed to the STORE/RECALL SETUP Menu.

d. Use the up or down cursor keys to position the cursor to user program numbers 0–9.

e. Enable the CLR softkey twice for each program number to clear each program from memory.

f. Proceed to the CONFIGURATION Menu and verify the USER PROGRAM reads PASS.

5. At the BERT SETUP Menu, perform setup procedures to perform selected test. If jitter testing is involved, proceed to display the JITTER SETUP Menu to select the desired jitter function or test setup.

6. Proceed to access the BERT RESULTS Menu. Select parameters to monitor for selected test.

7. Press the RUN/STOP key to start test. Verify the RUN LED is on.

8. Complete all 5500A setup procedures before making any connection to the circuit under test.

9. Any additional equipment used along with the 5500A can be connected at any time during the test.

3.1.1 Out–Of–Service Bit Error Rate Test

This is a test example using the 5500A to perform a BERT test on a circuit provisioned for AMI line coding and D4 framing format. This test can be performed in many ways. The distant end can be looped thru a CSU, Facility Loop Unit, or patch cord, where the data is looped back toward the test set. Another option is to do a end–to–end type test where another test set is at the distant end, transmitting and receiving the same test data.

Select the FRACTIONAL T1 BERT SETUP Menu and set the following test parameters.

BIT RATE	1.544Mbs	[S]
LINE CODE	AMI	
FRAME	D4	[X64]
PATTERN	QRW	
BLOCK SIZE	10^6	
BLOCKS	0	MON–DISABLED
BPV INJ RATE	1E–3	
LOGIC ERROR RATE	1E–3	
CLOCK SOURCE	INTERNAL	TERM–ENABLED
AUTO RESYNC	ENABLE	
TX ENA BDG/MON	DISABLE	
USER PAT SYNC	OFF	LOOP–DISABLED
BERT CHAN PAGE	DISPLAY	

Move the cursor to BERT CHAN display field, use the SELECT key to enable the BERT CHANNEL PAGE Menu. This menu is used to select the DS0's to be tested. A (X) beside the channel number indicates that the DS0 is selected for test. A (–) beside the channel number indicates that the DS0 is deselected. Channels that are deselected the idle code (all one's) signal is transmitted. To test the full bandwidth of the T1, select all 24 channels. To exit from the BERT CHANNEL PAGE, depress the down arrow menu key.

Go to the FRACTIONAL BERT RESULTS Menu and monitor the following parameters.

FREQUENCY (RC)	
RVR	BLK
BER	PF
ALRM	LOS
AHST	CRCE (ESF FRAMING ONLY)
FBE	ES
FBER	ET
LINE LEVEL can be monitored on the JITTER SETUP/ RESULTS Menu.	

Connect a test cord from the 5500A–636 RX jack to the LINE SIDE OUT jack (Figure 3–3).

Connect a test cord from the 5500A–636 TX jack to the LINE SIDE IN jack.

NOTE LINE IN and LINE OUT test toward the span. EQUIPMENT IN and OUT test toward the office equipment.

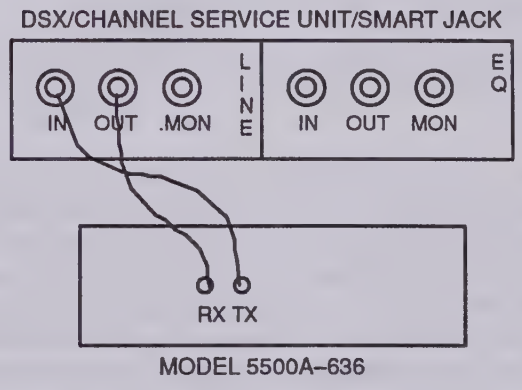

Figure 3–3. Out–of–Service Bit Error Rate Test Connections.

3.1.2 Clock/Frame Slip Test

This is an example using the 5500A to detect clock or frame slips, on a circuit provisioned for AMI line coding and D4 framing format. This test is a loop timing test that compares the RX clock against the T1 reference clock. Under ideal conditions no clock slips or frame slips should occur.

Select the FRACTIONAL T1 BERT SETUP Menu and set the following parameters.

BIT RATE	1.544Mbs	[S]
LINE CODE	AMI	
FRAME	D4	[X64]
PATTERN	QRW/NA	
BLOCK SIZE	10^6	
BLOCKS	0	MON–ENABLED
BPV INJ RATE	1E–3	
LOGIC ERROR RATE	1E–3	
CLOCK SOURCE	RX	TERM–DISABLED
AUTO RESYNC	ENABLE	
TX ENA BDG/MON	DISABLE	
USER PAT SYNC	OFF	LOOP–DISABLED
BERT CHAN PAGE	DISPLAY	

Move the cursor to BERT CHAN display field, use the SELECT key to enable the BERT CHANNEL PAGE menu. This menu is used to select the DS0's to be tested. A (X) beside the channel number indicates that the DS0 is selected for test. A (–) beside the channel number indicates that the DS0 is deselected. Channels that are deselected the idle code (all one's) signal is transmitted. To test the full bandwidth of the T1, select all 24 channels. To exit from the BERT CHANNEL PAGE, depress the down arrow menu key.

Go to the FRACTIONAL BERT RESULTS Menu and monitor the following parameters.

FREQUENCY (RC)	
CSLP	FSL
WND+	WND–
ALRM	FLOS
AHST	CRCE (ESF FRAMING ONLY)
FBE	ES
FBER	ET
LINE LEVEL can be monitored on the JITTER SETUP/RESULTS Menu.	

Connect a test cord from the 5500A–636 RX jack to the LINE IN MONITOR jack (Figure 3–4).

Connect a test cord from the 5500A–636 TX jack to the EQUIPMENT SIDE MONITOR jack.

NOTE LINE IN and LINE OUT test toward the span. EQUIPMENT IN and OUT test toward the office equipment.

NOTE The TX jack is the reference jack for determining clock or frame slips of the signal in the RX jack.

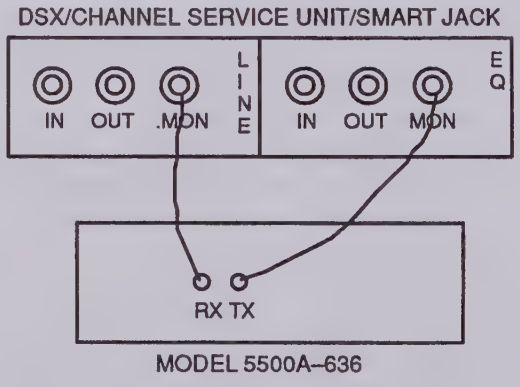

Figure 3–4. Clock/Frame Slip Test Connections.

3.1.3 In–Service Drop/Insert Test

This is a test example using the 5500A to drop a DS0(s) and insert a test pattern into selected channel(s). This test example assumes the circuit under test is provisioned for AMI line coding and D4 framing format. In the DROP/INSERT mode of operation the 5500A will not disrupt the live data on the unselected channels. But there will be a hit on the line once the test cord is connected to the circuit under test. The circuit should instantly receive and return to normal operation.

Select the FRACTIONAL T1 BERT SETUP Menu and set the following test parameters.

BIT RATE	1.544Mbs	[S]
LINE CODE	AMI	
FRAME	D4	[X64]
PATTERN	QRW	
BLOCK SIZE	10^6	
BLOCKS	0	MON–ENABLED
BPV INJ RATE	1E–3	
LOGIC ERROR RATE	1E–3	
CLOCK SOURCE	DROP/INS	TERM–DISABLED
AUTO RESYNC	ENABLE	
TX ENA BDG/MON	DISABLE	
USER PAT SYNC	OFF	LOOP–DISABLED
BERT CHAN PAGE	DISPLAY	

Move the cursor to the BERT CHAN display field, use the SELECT key to enable the BERT CHANNEL PAGE menu. This menu is used to select the DS0's to be tested. A (X) beside the channel number indicates that the DS0 is selected for test. A (–) beside the channel number indicates that the DS0 is deselected.

Go to the FRACTIONAL BERT RESULTS Menu and monitor the following parameters.

FREQUENCY (RC)	
RVR	BLK
BER	PF
ALRM	LOS
AHST	CRCE (ESF FRAMING ONLY)
FBE	ES
FBER	ET
LINE LEVEL can be monitored on the JITTER SETUP/RESULTS Menu.	

Connect a test cord from the 5500A–636 RX jack to the EQUIPMENT SIDE MONITOR jack (Figure 3–5).

Connect a test cord from the 5500A–636 TX jack to the LINE SIDE IN jack. (Performing this connection will cause a hit on the span.)

NOTE LINE IN and LINE OUT test toward the span. EQUIPMENT IN and OUT test toward the office equipment.

NOTE This operation places the selected data pattern into the selected DS0's only. All other DS0's should pass through unaltered.

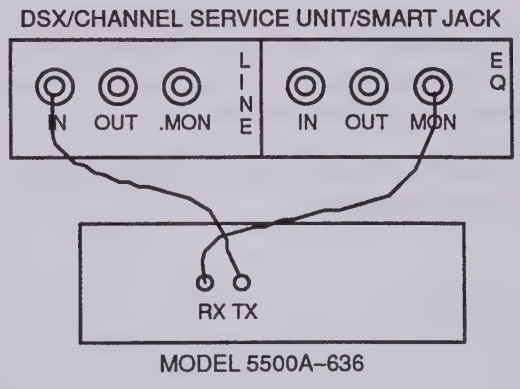

Figure 3–5. In–Service Drop/Insert Test Connections.

3.1.4 In–Service Monitor Test

This is an example using the 5500A to monitor an in–service T1 span. This test example assumes the circuit under test is provisioned for AMI line coding and D4 framing.

Select the FRACTIONAL T1 BERT SETUP Menu and set the following test parameters.

BIT RATE	1.544Mbs	[S]
LINE CODE	AMI	
FRAME	D4	[X64]
PATTERN	QRW/NA	
BLOCK SIZE	10^6	
BLOCKS	0	MON–ENABLED
BPV INJ RATE	1E–3	
LOGIC ERROR RATE	1E–3	
CLOCK SOURCE	Rx	TERM–DISABLED
AUTO RESYNC	ENABLE	
TX ENA BDG/MON	DISABLE	
USER PAT SYNC	OFF	LOOP–DISABLED
BERT CHAN PAGE	DISPLAY	

Move the cursor to the BERT CHAN display field, use the SELECT key to enable the BERT CHANNEL PAGE Menu. This menu is used to select the DS0's to be tested. A (X) beside the channel number indicates that the DS0 is selected for test. A (–) beside the channel number indicates the DS0 is deselected. To test the full bandwidth of the T1, select all 24 channels. To exit from the BERT CHANNEL Menu, depress the down arrow menu key.

Go to the FRACTIONAL BERT RESULTS Menu and monitor the following parameters.

FREQUENCY (RC)	
RVR	FLOS
RVPV	15Z
ALRM	%1SD
AHST	CRCE (ESF FRAMING MODE ONLY)
FBE	CRER (ESF FRAMING MODE ONLY)
FBER	ET
LINE LEVEL can be monitored on the JITTER SETUP/RESULTS Menu.	

Connect a test cord from the 5500A–636 RX jack to the LINE SIDE MONITOR jack (Figure 3–6).

NOTE LINE IN and LINE OUT test toward the span. EQUIPMENT IN and OUT test toward the office equipment.

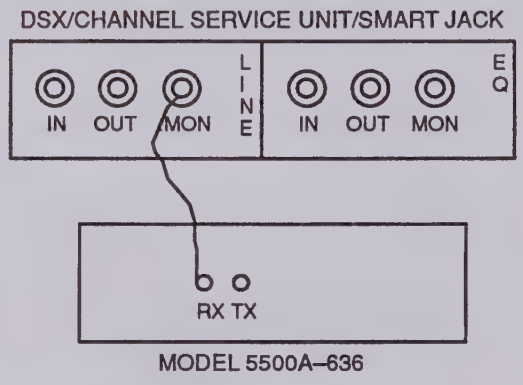

Figure 3–6. In–Service Monitor Test Connection.

3.1.5 DCE BERT Test

This is an example using the 5500A to test a DCE device (DSU/CSU's, modems, multiplexers, etc.). This test procedure is applicable for 5500–200, 5500–450, and V.35 interface modules.

Select the BERT SETUP Menu and set the following test parameters. (Select DTE simulation using the DCE/DTE key on the front panel. The choice will be displayed in the top left corner of the CRT.)

DTE–MODE		
TOD	– – – – – –	
CLOCK INV	TC. RC. XC.	FLOW
DATA INVET	TD. RD.	[OFF]
BIT RATE	EXT CLK	[S]
MODE	SYNC	
DCE SYN TD CLK	XC	
CHAR SIZE	– – –	
PARITY	– – –	
STOP BITS	– – –	
PATTERN	2047	
BLOCK SIZE	10^3	
BLOCKS	0	
AUTO RESYNC	ENABLE	LOOP–DISABLED

Go to the BERT RESULTS Menu and monitor the following parameters.

FREQUENCY (RC)	
BE	BLE
BER	BURS
BLK	ET
LOS	EFS

Connect a test cable from either the DCE or DTE port on interface module to device under test (Figure 3–7). (DTE and DCE ports are connected in parallel on 5500–200, 5500–450, and V.35 interface modules.)

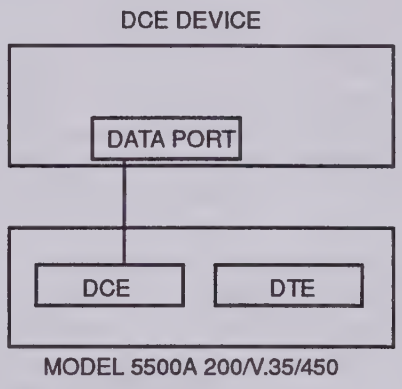

Figure 3–7. DCE BERT Test.

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Chapter 4 – Parameter Descriptions

4.0 INTRODUCTION

This section of the manual provides descriptions of parameters displayed on the Model 5500A test set menus.

Bit Error Rate Testing, whether at 75 bps rates or 1.544 Mbps rates, has a common purpose in digital circuit maintenance. That purpose is to determine whether or not a given transmission path can support a digital transmission without errors.

To test a digital circuit and determine whether or not errors are being generated, it is customary to employ a test set which generates and transmits a known pattern over the circuit. The circuit may be "looped" at the distant end or another test set may be located there. In any event, the pattern received is compared bit–by–bit to the known pattern generated and any discrepancies in the received pattern are counted as errors.

Since a known pattern must be substituted for the live traffic in order to perform a Bit Error test, these tests are often referred to as "out–of–service" tests.

The test patterns employed are pseudorandom or user sequences of binary digits which simulate live traffic. The term "pseudorandom" implies that the stream of bits only appears to be random. While the test pattern bit stream must appear to be random to simulate live traffic, it still must have some repetition in order for the test set to detect and recover the pattern.

Other patterns are useful for test purposes. The 5500A provides a pattern generator capable of generating pseudorandom sequences and USER input patterns as described in section 2 of this manual.

The variety of digital equipment to be tested, both DCE and DTE, is so vast that the choice of pattern depends upon a number of factors. For example, a pseudorandom sequence 63 bits long is suitable for low speed modem testing. At 300 baud or even 1200 baud, the 63 pattern looks like regular traffic. However, if we attempted to use this pattern at higher data rates (T1 for example) then the "random–like" nature of this pattern would disappear. It is also possible that certain pseudorandom sequences may generate long strings of zeros. Some systems have real problems with long strings of zeros. In particular, T1 carrier systems operating at 1.544 Mbps, restrict data patterns to no more than 14 consecutive zeros.

As a rule of thumb, the choice of patterns follows the bit rate of the device or system under test. The higher the bit rate the longer the pattern and vice versa. Thus we see 511 patterns used for testing 1200 baud modems and the QRW used to test T–carrier systems.

The 5500A test set provides the tool for analyzing the symptoms of the problem and, if possible, increases the diagnostic ability of the technician by providing him with accurate information. The 5500A measures and displays up to twenty–seven error parameters plus bias distortion, frequency, event, time, and optional jitter simultaneously. The 5500A places all of the analysis tools in one instrument and provides all of the test results simultaneously. This improves the user's ability to solve problems faster because the 5500A can simulate the problems (inject errors or jitter) and analyze the symptoms simultaneously.

4.1 BERT DISPLAY OPTION DEFINITIONS

The following definitions of the BERT parameters provide an understanding of what is being measured and how it is being measured.

ABE Adjusted bit errors differ from the standard bit error function. Adjusted bit errors include, in addition to the standard in synchronization errors, an error count equal to one half the bit rate. For example, a unit may have the following totals:

Frequency = 1.544MHz
BE = 12
SLS = 0.25
ABE = 193012
ETS = 10
EFS = 9.45

The ABE parameter is calculated by taking the total BE (12), plus one half the bit rate (1.544E06/2), times the amount of time in sync loss (0.25), equals:

$$ABE = 12 + 0.25\,\frac{1,544,000}{2} = 193012$$

ABER Adjusted bit error rate. The adjusted bit error rate is calculated in a manner similar to bit error rate. The adjusted bit error rate is the number of adjusted bit errors divided by the total number of bits. From the example given in the ABE definition:

$$ABER = \frac{ABE}{Bits + (SLS \times Bit\ Rate)}$$

AES Available errored seconds. The number of seconds, in available time, that are errored.

AHST Alarm history. The alarm display is a real time display and will indicate the presence of an alarm only when the alarm condition is present. The alarm history display is a record of any alarms that have occurred during the test period regardless of their current state. The alarm history format is the same as the alarm format.

ALRM Alarms. This parameter provides the user with information on the current, real time status of the receive side of the system under test and is available with the Model 5500–624 Framed T1 Interface and 5500–628 (636) ESF T1 Interface Options. Four or five alarm states are displayed in this block. The alarm states for the 5500–624 module are as follows.

The first alarm is B2. This is the so–called YELLOW ALARM. It means that bit number 2, in each of the twenty four received PCM channels making up to the T–Carrier, was forced to zero for more than 50 milliseconds. This indicates that the terminal equipment at the remote end of the circuit has lost synchronization or that there has been no incoming DS–1 data for more than two seconds.

The second state is indicated by an S. This character, when present on the display, indicates that signaling frame bit errors are occurring. The T–Carrier framing format is an interleaved pattern twelve bits in length. Six of these bits are signaling frame bits while the other six bits are terminal frame bits. The occurrence of 2 out of 4 or 2 out of 5 frame bits in error will cause the terminal to try to resync. This can propagate a burst of errors down the line.

The third state, loss of PCM, is indicated by a C on the ALRM display block. If a string of 14 or more consecutive zeros is received, or if no data transitions occur for 2 or more seconds, the C indication is displayed.

The fourth state is indicated by an F on the ALRM display. This indicates that errors in the terminal framing bits are occurring.

The presence of one or more of these four characters on the ALRM display indicates an abnormal condition which must be investigated and cleared before continuing with any error testing.

The normal indication on the ALRM display is an all dots pattern (.....). The four states occupy the following positions (Y.B.C.S.F), and any one or all could be present at one time. These are qualitative and not quantitative indications. It is more important to know that these conditions exist than it is to count how often they occur (refer to section 2 for the ALRM display for the 5500A–628 or 636 module).

BALS Blue Alarm. A blue alarm (all ones) is a response by the DTE to the detection of a loss of signal. A blue alarm is also referred to as an Alarm Indication Signal (AIS). The 5500A detects blue alarms and reports them as blue alarm seconds. A blue alarm second is defined as a one second interval in which there was at least one blue alarm detected.

BE Bit Errors. The known generated pattern is compared, by the detector, to the received pattern on a bit–by–bit basis. Any received bit

pattern on a bit–by–bit basis. Any received bit which does not agree with what is known to have been sent is counted as an error. The error data is accumulated in a 16–bit register which is accessed by the processor every 1 millisecond. No error occurrences can be left undetected to a probability of 1x10–16.

BER Bit Error Rate. The 5500A is capable of providing the user with a bit error rate calculated as a running average or a one time event. The continuous moving average bit error rate changes as the number of bits received increases. This provides the user with a running indication of the "health" of the circuit under test at all times rather than forcing the user to set in a number of bits, wait for the unit to process the data, calculate a BER number for the test length, and wait to be restarted to measure BER again.

The user can, of course, force the 5500A to emulate other test sets by choosing a combination of block length and number of blocks in a test to yield a specific bit length test.

For example, assume that the user desires to have the 5500A compute BER for a test length of 10^5 bits. Choose a block length of 10^3 bits/block and 100 blocks for the number of blocks to be tested and you have a total of 10^5 bits. Press RUN and at the end of the 10^5 bits the 5500A will stop. At that time the BER block will have a numerical result which is the BER for the 10^5 BITS. Of course the user could obtain 10^5 bits by using a 10^4 block size and 10 blocks to test or a 10^5 block size and 1 block to test.

The Bit Error Rate is calculated based upon the bit errors and number of bits received. The 5500A is capable of providing this calculation on an ongoing basis (running average) or a one time basis. The advantage of the running average bit error rate is that it allows the user to track the ups and downs as the test progresses rather than have to wait until the end of the test to get an answer.

$$BER = \frac{Bit\ Errors}{Number\ of\ Bits\ Received}$$

The BER is updated at least once per second while testing is underway, since this is the minimum update rate of the CRT.

BITS Received Data Bits. This parameter is presented in scientific notation as, for example, 3.9E06 which means 3.9 million bits have been received.

BLE Errored Blocks. This is the number of blocks received with at least one bit in error. A block error will be counted whether one error or fifty errors occurs during the block.

BLE Block Error Percent. This is the number of running blocks received, divided by the number of errored blocks.

$$BLE\% = \frac{\#\ Blocks\ Received}{BLE}\ 100$$

BLK Blocks. This is the number of blocks received by the 5500A. This number steadily accumulates during a test and is composed of all blocks both errored and error free. Setting the block length on the 5500A (10@ to 10) determines what the receiver looks for and calls a block. The 5500A will start to count blocks when it is running and has acquired sync.

BURS Burst Errors. A burst error event is a number of bit errors occurring over a short period of time (one block) and grouped so closely that they are seen as "one event". The number of consecutive bit errors that define the beginning of a burst and the number of consecutive error free bits that define the end of a burst are user programmable.

CBE Current Bit Error. The current bit error parameter is the number of bit errors that have occurred over the immediate past five seconds. This gives the user a measure of recent bit errors to aid in determining if adjustments to the transmission facilities are having an immediate effect.

CBER Current Bit Error Rate. The current bit error rate is a measure of the bit error rate over the last five seconds. If a burst of errors occurs, the current bit error rate should register the number of bit errors in the last five seconds divided by the number of bits in the last five seconds.

CEFS CRC Error Free Seconds. CRC error free seconds are defined in the 5500A as the number of seconds that have elapsed that contained no CRC–6 errors. The formula used for calculating CRC error free seconds by the 5500A is:

$$CEFS = ETS - CRES$$

CFS% Percent of CRC Error Free Seconds. The percent of CRC error free seconds is a ratio of CRC error free seconds to total elapsed seconds. It is computed as:

$$\%CFS = \frac{CFS}{ETS}\ 100$$

CODE Last Bpv Code Received.

CR4EFS CRC4 Error Free Seconds. CRC4 error free seconds are defined in the 5500A as the number of seconds that have elapsed that contained no CRC–4 errors. The formula used for calculating CRC4 error free seconds by the 5500A is:

$$CR4EFS = ETS - CR4ERS$$

CR4ERR CRC4 Errors. CRC–4 (cyclic redundancy check) errors can be detected on either in–service or out–of–service CEPT lines. CRC–4 uses a mathematical algorithm to check the contents of the frame and results in a 4–bit code. The CRC code of each frame is encoded as 4–bits in the following frame. As each frame is received and decoded, a CRC check is recalculated and compared to the CRC code that was sent over the span. If they do not match, then one or more errors occurred during transmission of the frame.

As CRC–4 errors occur they are counted in a binary counter. This counter is read every 20 milliseconds and the count is accumulated as a 48–bit binary number for reporting in the CRCERR field of the 5500–836 Bert Menu.

CRC4RS A CRC errored second is defined as a one second window in which at least one CRC error occurred. CRC errored seconds in the 5500A are measured synchronously, which means a CRC error initiates the errored seconds timer.

CR4FS% The percent of CRC error free seconds is a ratio of CRC error free seconds to total elapsed seconds. It is computed as:

$$\%CR4FS = \frac{CR4EFS}{ETS}\ 100$$

CR4RAT One more category pertaining to CRC–4 errors has been defined as CR4ERR/ES or CRC errors per CRC errored second. This parameter is nothing more than the number of CRC errors that occurred in the last CRC errored second. Its primary use is to print to an external printer the number of CRC errors that occurred within every CRC errored second. These numbers could then be tabulated to characterize the occurrences and frequency that CRC errors occurred.

CRCE CRC Errors. CRC–6 (cyclic redundancy check) errors can be detected on either in–service or out–of–service lines employing the extended superframe (ESF) mode of framing. CRC–6 uses a mathematical algorithm to check the contents of a extended superframe and results in a 6–bit code for the extended superframe. The CRC code of each extended superframe is encoded as 6 bits in the following extended superframe. As each extended superframe is received and decoded, a CRC check is recalculated and compared to the CRC code that was sent over the span. If they do not match, then one or more errors occurred during transmission of the extended superframe.

As CRC–6 errors occur they are counted in a 16–bit binary counter. This counter is read every 20 milliseconds and the count is accumulated as a 48–bit binary number for reporting in the CRCE field of the 5500–628 Bert Menu.

CRER CRC Error Rate. One more category pertaining to CRC–6 errors has been defined as CRCER/ES or CRC errors per CRC errored second. This parameter is nothing more than the number of CRC errors that occurred in the last CRC errored second. Its primary use is to print to an external printer the number of CRC errors that occurred within every CRC errored second. These numbers could then be tabulated to

characterize the occurrences and frequency that CRC errors occurred.

CRES CRC Errored Seconds. A CRC errored second is defined as a one second window in which at least one CRC error occurred. CRC errored seconds in the 5500A are measured synchronously, which means a CRC error initiates the errored seconds timer. CRC errored seconds are available only during the ESF mode of operation.

Where ETS is the total number of elapsed test seconds and CRES is errored seconds as described above.

CSLP Clock Slip. All timing information is transmitted isochronously as part of the 1.544 Mbps bipolar signal. Isochronous timing indicates that a clock is extracted from the incoming signal and is used to provide timing to the outgoing signal. A slip is defined as the overrun or under run of 193 bits, or one frame. If one frame of storage is provided, slips will occur approximately as follows. One extra bit in every one billion bits would cause a slip every two weeks at 1.544 Mbps. One in one million would cause slips 1000 times more frequently, or a slip about every half hour.

EBR Errored Block Rate. The 5500A provides the user with a block error rate calculated as a running average. The continuous moving average block error rate changes as the number of blocks received increases. This provides the user with a running indication of the "health" of the circuit under test at all times, rather than forcing the user to set in a number of bits, wait for the unit to process the data, calculate a EBR number for the test length, and wait to be restarted to measure EBR again.

ED Errored Days. The number of days during which at least one bit error occurred. Useful in very long term testing or when testing in accordance with certain European specifications such as CCITT G.821.

EFB Error Free Blocks. This is the number of blocks received without an error in them and is calculated as:

$$BLKS - ERRORED\ BLKS = ERROR\ FREE\ BLKS$$

EFS Error Free Seconds. This important parameter is often used to characterize a data link. It is defined as the number of seconds during which no errors have occurred. It is counted by the 5500A when the unit is running and has acquired sync. The total of ES plus EFS is equal to the ETS.

EFS% Percent of Error Free Seconds. The percent of error free seconds is a ratio of error free seconds to total elapsed seconds. It is computed as:

$$\%EFS = \frac{EFS}{ETS}\ 100$$

ES Errored Seconds. An error second has occurred if at least one error occurs in the one second interval. The 5500A measures "synchronous" errored seconds (a bit error event initiates the errored second timer). Errored seconds, like all measurements, will start to be accumulated by the 5500A when it has begun to RUN and it has acquired sync.

ESR Errored Seconds Rate. This is the number of errored seconds divided by the number of seconds and is a moving average.

$$ESR = \frac{ES}{ETS} = \frac{ES}{ES + EFS}$$

This parameter can easily yield other qualitative results for the user. In particular, the user can derive the % of Errored Seconds and % of Error Free Seconds quite easily from ESR. To obtain the percent errored seconds, simply multiply the numerical result in the ESR display window by 100. For example, assume the reading for ESR is 3.1 E–2. Multiplying .031 by 100 yields the result 3.1% Errored Seconds. The percent error free seconds can be easily calculated by subtracting the 3.1% from 100% which yields 96.9% error free seconds.

ET Elapsed Time. This is the elapsed test time in hours/minutes/seconds since the RUN/STOP

switch was set to RUN and the 5500A acquired sync. Elapsed time will not accumulate if the unit is not in sync or during sync losses.

ETS Elapsed Time in Seconds. This is the elapsed test time given in total seconds as opposed to the hours/minutes/seconds given by ET.

FBE Frame Bit Errors. Frame bit errors are detected by the 5500A by comparing the input data stream to the known FT frame bit sequence. The frame bit sequence is a result of adding one frame bit every 192 information bits. Violations of the frame bit sequence within the superframe are declared as frame bit errors and are counted in a 16–bit binary counter.

This counter is read every 20 milliseconds and the count is accumulated as a 48–bit binary number for reporting in the FBE field of the 5500A–628 Bert Menu.

FBER Frame Bit Error Rate. The frame bit error rate is defined as the rate at which FT framing errors are being detected. Unlike bit error rates which can only be determined on known bit patterns, the 5500A can provide the user with a continuous frame bit error rate, regardless of the data but only for framed data, which changes as the number of frame bits received changes. This continually changing rate provides the user with a constant indication of the "health" of the line under test.

The frame bit error rate is calculated by the 5500A using the following formula:

$$FBER = \frac{Frame\ Bit\ Errors}{Total\ FT\ Bits\ Received}$$

FBES Frame Bit Errored Seconds. A frame bit errored second is defined as a one second window in which at least one FT frame bit error occurred. Frame bit errored seconds in the 5500A are measured synchronously (a framing error initiates the errored seconds timer). Frame bit errored seconds are available during all framed modes of operation.

FEFS Frame Bit Error Free Seconds. Frame bit error free seconds is another measure of the performance level of a circuit using some form of framing, either D4 or ESF. It is defined as the difference of total elapsed test seconds minus the frame bit errored seconds that occurred over the total test seconds and is calculated by the 5500A using the formula:

$$FEFS = ETS - FBES$$

In this case, ETS is the total number of seconds of testing regardless of pattern sync.

FFS% Percent Frame Bit Error Free Seconds. The percent of frame bit error free seconds is a ratio of frame bit error free seconds to total elapsed seconds. It is computed as:

$$\%FFS = \frac{FFS}{ETS}\ 100$$

FLOS Frame Sync Loss. A signal is in frame sync if not more than 2 out of 5 Ft bits are in error. It is out of sync if 2 or more out of 5 Ft bits are in error.

When frame sync is lost, the loss is counted by a 16–bit counter which is read every 20 milliseconds and accumulated in a 48–bit register for long term storage. Since the software can only get around to check the frame sync status every 20 milliseconds, it assumes that all sync losses that may have actually been of a much shorter duration, to be a loss of 20 milliseconds. The parameter displayed for the user pertaining to frame sync is Frame Sync Losses (FLOS) and is incremented every time frame sync is lost.

FLS Frame Loss Seconds. The frame loss seconds parameter is provided for T1/T1C modules. It is a measure of the number of seconds the data has been unframed. Frame loss seconds measures down to 0.01 seconds and displays three significant digits. Therefore, 10.14 would be displayed as 10.1 seconds.

LOOP TIMING Loop timing was implemented in the 5500–628 (636) interface module in order to tell the user whether the circuit under test is loop timed. All timing information is transmitted isochronously as part of the 1.544 Mbps bipolar

signal. Isochronous timing indicates that a clock is extracted from the incoming signal and is used to provide timing to the outgoing signal. A loop timed circuit is defined as frequency locking the oscillators which clock the outgoing 1.544 Mbps signal to the long term average frequency of the incoming 1.544 Mbps signal. An advantage of a loop timed circuit is the reduction in the number of frame slips that occur when a receiving device receives a signal of one frequency and then re–transmits at a slightly different frequency.

A slip is defined as the overrun or under run of 193 bits, or one frame. If one frame of storage is provided, slips will occur approximately as follows. One extra bit in every one billion bits would cause a slip every two weeks at 1.544 Mbps. One in one million would cause slips 1000 times more frequently, or a slip about every half hour.

The received signal has its clock extracted from the signal as a normal mode of operation. The signal present at the transmit side of the 5500A also has its clock extracted from it. These two clocks are then each fed into a 16–bit free running counter. Upon power–up and immediately after a clear sequence, the software latches both counters simultaneously and reads the current counter values. From these two values an initial delta (DELTA1) is computed which becomes a reference point. DELTA1 is also stored as DELTA1 from which comparisons are made. From then on, until another clear is encountered, the two counters are read every 20 milliseconds and additional delta (DELTA2) is computed.

The two deltas (DELTA1 and DELTA2) are then compared. If they are the same or have not deviated by more than 40 clock counts, the circuit is assumed to be loop timed. If they are different by more than 40 counts, the circuit is not loop timed.

The CSLP (Clock Slip) parameter is simply the rate at which the two clocks are changing. The 5500A divides the current clock count by the total elapsed test seconds to derive the slip rate. The units for slip rate are thus counts per second.

Two other parameters are defined as WANDER+ and WANDER–. These parameters are the maximum positive clock count and the maximum negative clock count, respectively. If a circuit is loop timed but has some amount of wander (defined as jitter less than 10 Hz), these two parameters will show that amount deviating at the reference point. If a circuit is definitely not loop timed, then one or the other wander parameters will constantly change at the same rate and direction.

LOS Loss of Sync. This parameter is based upon a bit error rate threshold being crossed. That is, when the bit error rate becomes excessively high, the 5500A will at some point, declare that it has lost sync and will not recover sync until the bit error rate drops below the threshold. The sync loss threshold in the 5500A is adjustable. It is factory set for initiating a sync loss whenever any 1000 bits received contains 100 or more errors. That is a BER 10–1 or higher. When the 5500A is out of sync, error parameter collection is meaningless. Only the time the unit is out of sync is accumulated.

MDY Month/Day/Year. The month, day, and year are available to date stamp any events printed out. The setting is retained in non–volatile memory. The settings are changed like any other parameters from the BERT Setup Menu. These settings should be reviewed to account for leap year or other factors affecting the read out.

%1sD Percent One's Density. The percent one's density is provided for T1/T1C modules and is a ratio of the number of one's bits to the total number of bits. It is displayed as a percentage and will display in inverse video if the density drops below 12.5%. An alternate pattern should yield about a 50% one's density.

PSL+, PSL– Pattern Slips. The 5500A detects pattern slips and records the amount of slippage up to 20 bits in either direction. Pattern slippage is displayed as two parameters, PSL+ and PSL–, which are the positive and negative pattern slip magnitudes in units of bit intervals.

A pattern slip occurs when a bit is replicated in the pattern or when a bit is removed from the pattern. An example is shown below:

```
1 1 0 0 1 1 1  original pattern

1 1 1 0 0 1 1 1 added bit

1 0 0 1 1 1   missing bit
  ^
```

PF Power Failures. The 5500A counts power failures to its input power supply. The threshold for counting a power failure is 90 volts ac (180 volts ac if operating from a 220–240 Vac source) or less. This enables the operator to determine whether or not ac power was continuously available during long term unattended tests. Upon powering up the 5500A, a power failure will be indicated, so the user should always press the CLEAR "softkey" at the lower right of the main BERT CRT display before doing any testing.

RBPV Receive Bipolar Violations. These are bipolar violations of the AMI line code which occur on the receive pair. Unlike the TBPV parameter, BPV's on the receive side of the line can be measured when the 5500A is operating in the TERMINATED mode as well as the BRIDGE mode.

RVFS Receive Violation Free Seconds. The count of the number of seconds on which no violations occurred on the receive pair of the T–Carrier under test.

RVR Receive Violation Rate. The rate at which receive BPV's occur. The RVR parameter can be measured in both the BRIDGED and TERMINATED modes. It is calculated as:

$$RVR = \frac{RBPV\ (violation/bit)}{number\ of\ bits}$$

RVS Receive Violation Seconds. This is a count of each second in which at least one receive violation occurs.

SES Severely errored seconds. Seconds that are characterized by a high error ratio (STHR). The value specified in the G.821 definition is .001 (1 bit error in every 1000 bits), but due to the fact that customers need to be able to set this threshold (STHR) to a lower value, the 5500A allows the operator to specify the number of errors (STHR) that determines a SES.

SLS Sync Loss Seconds. This represents the total accumulated time the unit is out of sync. A single sync loss of very short duration (much less than 1 second) will not cause the SLS counter to record. The sync loss itself will be counted but a sync loss second is not necessarily counted. The counter will, however, accumulate the outage time so that, for example, if each sync loss had a duration of 200 milliseconds, then after 5 such occurrences, the counter would increment and display a 1 in the SLS block. It is important to note that the information is not lost but only waiting for the total outage to reach 1 second.

TBPV Transmit Bipolar Violations. This parameter is the count of violations of the Alternate Mark Inversion (AMI) bipolar line code format used for T1 and T1C transmission in the U.S. In this case, the BPV's are being monitored on the transmit pair of four wire T–Carrier system, hence the designation TBPV. This parameter is only measured by the Model 5500–600 module option operating in the Bridge Mode. In this mode this interface option has two receivers active and can monitor both the transmit pair and the receive pair of a full duplex T–Carrier. Transmit line bipolar violations, TBPV, may be measured in the BRIDGE mode, or may be injected at a programmed rate (but not measured) in the TERMINATE mode when the 5500A transmitter is enabled.

TOD Time of Day. The time of day in hours, minutes, and seconds is available to time stamp any events printed out. The setting is retained in nonvolatile memory.

TVFS Transmit Violation Free Seconds. The number of seconds without a bipolar violation. The sum of TVS and TVFS equals the elapsed time in seconds (ETS).

TVR Transmit Violation Rate. The rate at which transmit BPV's occur. The TVR parameter can be measured only in the BRIDGED mode. It is calculated as:

$$TVR = \frac{TBPV}{number\ of\ bits}\ (violations/second)$$

TVS Transmit Violation Seconds. This is a count of each second in which at least one bipolar violation occurs. It is similar in usage to errored seconds (ES).

WND+ Wander Positive. Two parameters defined as WANDER+ and WANDER– are the maximum positive clock count and the maximum negative clock count, respectively. If a circuit is loop timed but has some amount of wander (defined as jitter less than 10 Hz), these two parameters will show that amount deviating at the reference point. If a circuit is definitely not loop timed, then one or the other wander parameters will constantly change at the same rate and direction.

WND– Wander Negative. Two parameters defined as WANDER+ and WANDER– are the maximum positive clock count and the maximum negative clock count, respectively. If a circuit is loop timed but has some amount of wander (defined as jitter less than 10 Hz), these two parameters will show that amount deviating at the reference point. If a circuit is definitely not loop timed, then one or the other wander parameters will constantly change at the same rate and direction.

YALS Yellow Alarm Seconds. A yellow alarm is the result of a customer's terminal equipment not being able to synchronize on the DS1 signal from the network. In response to this failure, the terminal equipment must issue a yellow alarm. Also, equipment recognizing a red alarm (out–of–frame condition for 2.5 seconds or more) should transmit a yellow alarm in the opposite direction.

A yellow alarm is indicated in D4 framing mode by setting bit 2 of 255 consecutive channels to a zero. In the ESF mode, a yellow alarm is indicated by 16 ± 1 sets of alternating eight 1's / eight 0's pattern in the 4 Kbps data link.

The 5500A detects yellow alarms in both modes of framing and reports them as yellow alarm seconds (YALS). A yellow alarm second is defined as a one second interval in which there was at least one yellow alarm detected.

>15Z 15 zeros is a measure of the number of times the T1 bit stream has contained 16 or more consecutive zeros.

15ZS 15 zeros seconds is the count of the number of seconds that have had one or more 15 zeros condition.

4.2 G.821 DEFINITIONS

The G.821 parameters are defined in paragraph 6.2 of section 6 in this manual.

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Chapter 5 – Remote Operation

5.0 INTRODUCTION

This section of the manual provides remote operation information for the 5500A test set.

The 5500A remote control ports permit the user to control the 5500A from a computer or dumb terminal. Both IEEE–488 and RS–232 ports are provided. Both connectors are located on the rear panel of the 5500A. Before connecting the 5500A to one of the remote ports, the remote port must be selected and the remote port characteristics must be configured to match the computer or terminal characteristics.

5.1 REMOTE PRINTER PORT CONFIGURATION

The 5500A RS–232 remote port is capable of connecting to either a DCE (Data Circuit–Terminating Equipment) or a DTE (Data Terminal Equipment) type device. There are 6 selector (3 sets of 2) switches on the 5500A control board that must be configured to permit the 5500A to communicate with the device connected to the port.

NOTE A DTE device must be connected to a DCE device and vice–versa.

To gain access to these switches, the top cover of the 5500A must be removed. This is accomplished by removing the 2 screws holding the top rear retaining bezel, and then sliding the top cover and bezel back to expose the 5500A control board.The three sets of switches are mounted on the control board, near the RS–232 port, as shown in Figure 5–1. Each switch has DCE and DTE printed on the board. If a data terminal equipment (DTE) device, such as a printer or CRT is connected to the RS–232 port, then set all the switches to DCE so the 5500A appears as a DCE device. Likewise, if a data circuit–terminating equipment (DCE) device, such as a modem, is connected to the RS–232 port, then all the switches must be set to DTE so the 5500A appears as a DTE device. Table 5–1 lists the interface signals and their function for DCE and DTE with the corresponding pin assignments.

5.2 INITIAL SETUP

Select the RS–232/IEEE–488 menu on the 5500A (refer to Figure 5–2). This menu is used to configure the 5500A to match those of the terminal or computer to be used as the remote control device. Enabling the TRACE on the menu permits the user to monitor the character data streams across the RS–232 bus. Data from the terminal will appear on the left side of the screen on the second line (line with the "] [" in the center) while the data from the 5500A to the communicating device will appear on the same line to the right.

The 5500A supports four modes of protocol:

1. IEEE488 CR–LF

2. IEEE488 ACK

3. RS232 CR–LF

4. RS232 ACK

   a) IEEE–488/CRLF

1. Install the GPIB card in your computer and configure the software as described by National Instruments installation procedure.

2. Run "IBCONF" on your computer and change the configuration of "GBIB0" as follows:

   Primary GPIB Address 0
   Secondary GPIB Address ..... NONE
   Timeout Setting T10s
   EOS Byte 0DH
   Terminate Read on EOS ..... NO
   Set EOI with EOS on Write ..... YES
   Type of compare on EOS 7–bit
   Set EOI with last byte of write ..... NO

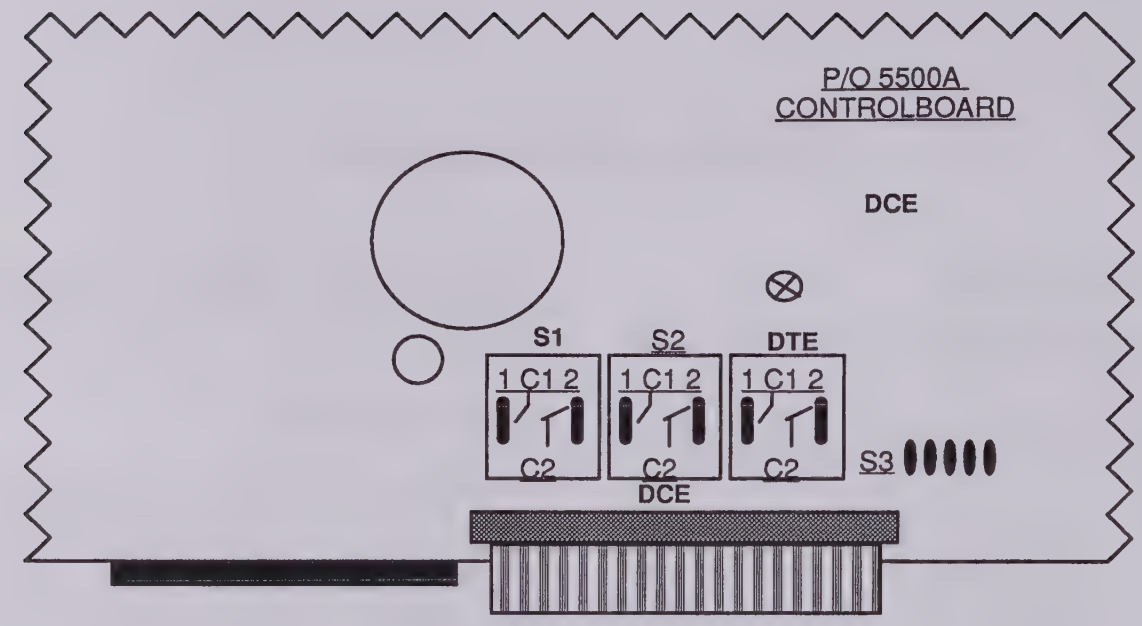

Figure 5–1. DCE–DTE Select Switches on 5500A Control Board.

Table 5–1. Remote Port Pin Functions.

PIN	FUNCTION		SOURCE	
	DTE	DCE	DTE	DCE
2	TXD	TXD	5500	USER
3	RXD	RXD	USER	5500
4	RTS	RTS	5500	USER
5	CTS	CTS	USER	5500
6	DSR	DSR	USER	5500
7	Sig GND	Sig GND	———	———
8	DCD	DTR	USER	USER
20	DTR	———	5500	———

GPIB–PC Model PC2
Board is System Controller ..... YES
Local Lockout on all devices ..... YES
Disable Auto Serial Polling ..... YES
Disable Device Unaddressing ..... NO
High Speed Timing ..... NO
Interrupt Jumper Setting ..... NONE
Base I/O Address ..... (2B8H)
DMA Channel ..... NONE
Internal Clock (in MHZ) 8

When the controller (PC) is configured as a talker (TE) and the 5500A is configured as a listener (LE), an absolute terminator <CR> carriage return will be sent by the talker. For example, <COMMAND> <CR>, the EOS byte will be sent by the talker along with EOI to the listener. The listener (5500A) recognizes that this is a command and will respond accordingly. Do not attempt to terminate commands with characters other than a <CR> as unpredictable results may be experienced.

3. Configure the 5500A as devices in "IBCONF". The recommended setup is as follows:

Primary GPIB Address	<user defined>
Secondary GPIB Address	NONE
Timeout Setting	T10s
EOS Byte	0DH
Terminate Read on EOS	NO
Set EOI with EOS on Write	YES
Type of compare on EOS	7–bit
Set EOI with last byte of write	NO

Note that when the 5500A is configured as a talker (TE) and the controller (PC) is configured as a listener (LE), the 5500A sends a **unique** terminator with EOI, i.e., <RESPONSE> CR LF 00H. This unique terminator is a null character (00H) and is reflected by a "Z" character in the trace display on the 5500A. False terminators have been experienced with certain IEEE488 controllers because we have embedded <LF> throughout our response messages. Therefore it was necessary to create an unique terminator. This protocol is only valid with software revision 7.04 or higher.

b) IEEE–488/ACK

Unlike the previous mode, in which the controller operated in an open loop manner, the ACK protocol provides a response to each command regardless of whether the command returns data. If the command is understood, an ACK (06H) character is returned. If an error is encountered in interpreting the command, NAK (15H) is returned. If additional data is to be returned, it follows the first ACK and is terminated by a second ACK. Three possible responses are shown below:

(error)	NAK	EOI
(good, no data)	ACK	EOI
(good, data)ACK		
	Char 1	
	"	
	"	
Char x		
ACK	EOI	

In all cases the EOI line indicates end of response.

c) RS232/ACK

Operation of the RS–232/ACK protocol is identical to the IEEE–488 protocol with the exception that there is no EOI line. It is the controllers responsibility to know whether or not additional data is expected following the first ACK. In practice, this knowledge comes naturally with the program organization.

This protocol uses a half–duplex data transfer structure on the RS–232 port. The 5500 controls data flow to itself through the DTR line and sends data via the RTS/CTS handshake.

d) RS–232/CRLF

This mode is intended primarily for use with a directly connected terminal. It operates full–duplex and echoes every character received. In this mode, DEL and <Back Space> send a character sequence, the response to which will delete the last character. A <Control X> will cause the 5500 to ignore the present line. If an error is encountered in interpreting the input line, it is reprinted to the error point and a question mark (?) is inserted. The response to the command is shown on the line following the command.

When a protocol has been selected, use the cursor movement, cursor select keys, and softkeys to make the Remote Port Configuration Menu, as shown in Figure 5–2, match the selected characteristics. In the example shown in Figure 5–2, RS–232 has been selected by pressing the top softkey. Then by using the cursor movement and cursor select keys, the TRACE mode was disabled, CR–LF protocol was selected, the Bit (Baud) Rate was set to 600 bps, the character size was set to 8, parity was set to none, and the number of stop bits was set to two.

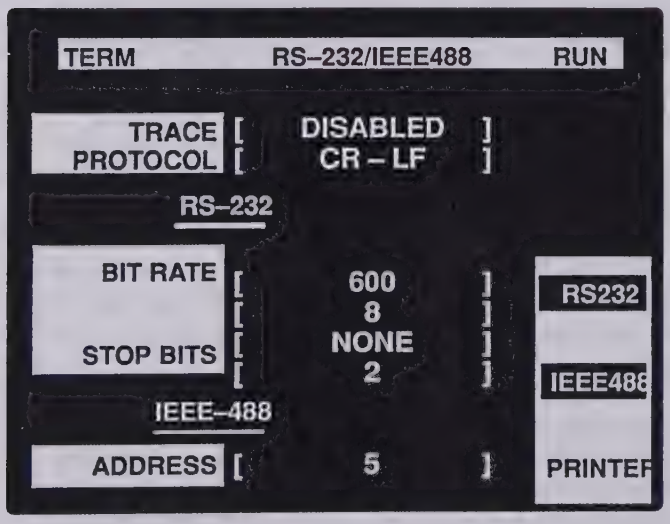

Figure 5–2. Model 5500A RS232/IEEE488 Menu.

5.3 ELECTRICAL CONNECTION

5.3.1 RS–232 Port

The 5500A is shipped from the factory with its RS–232 port configured as a DCE. That is, it is emulating a modem expecting a printer or terminal to be connected to it. If it is desired to connect a modem to the port, a null modem cable must be used, or the internal dip switches within the 5500A must be changed to the DTE position. Refer to section 2 of this manual for instructions regarding this change. The RS–232 port pin assignments are as follows:

PIN	FUNCTION	SOURCE
3	RD	USER
2	TD	5500A
5	CTS	USER
4	RTS	5500A
20	DTR	5500A
8	DCD	USER

5.3.2 IEEE–488 Port

The IEEE–488 Bus enables the simultaneous connection of up to 31 instruments to a single controller. The system operates by prefacing each data packet with an address. It is thus necessary for the user to select a numeric address (0–30) for the 5500A. Then it will 'listen' on the bus and respond to any commands prefaced by its address. The IEEE–488 port pin assignments are shown below:

PIN	FUNCTION	PIN	FUNCTION
1	D101	2	D102
3	D103	4	D104
5	E10	6	DAV
7	RFD	8	DAC
9	IFC	10	SRQ
11	ATN	12	CHASSIS
13	DIOS	14	D106
15	D107	16	D108
17	REN	18	GND
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND

5.4 COMMAND DESCRIPTION

Commands to the 5500A are divided into two basic types. The first command type, configuration commands, is used to configure the test setup. Commands of the second type, result commands, are used to read the test results. Configuration commands have three formats. The first format is the command issued by itself (for example BR for bit rate). When issued with no parameters, all of the configuration commands return their present setting. The second format is to follow the command with a question mark (?) in the parameter field (for example BR ?). In response to this format, the 5500A returns either a list of all possible settings for this command or a description of the parameter setting format. The third format is the command followed by a valid parameter. This results in the immediate update of the selected function to the specified state (for example BR 9600 sets the bit rate to 9600 bps).

The second command type, the results commands, is used to read test results. These commands ignore any data past the command field and always return the present value of the selected function. In most cases, the value returned in response to one of these commands is a snap–shot of the parameters value at the instant the command is evaluated. The exceptions to this are event time, frequency measurement, and bias. These three measurements are configured such that repeated requests will result in a newly measured value for each response. This allows for the gathering of meaningful data in cases where statistical analysis will be done on the readings.

NOTE This can result in response delays of up to 10 seconds when reading event times and approximately one second when reading either frequency or bias.

In addition to the command types described above, certain commands are dependent upon the type of interface. These are divided into commands which function with all interface modules, those which function only with the T1/T1C interface, and those which function with any interface other than T1/T1C. In the following tables which define all the commands, this is noted with an ALL for all, T1/T1C for T1/T1C only, OTHER for other than T1/T1C and specific module name where command is only applicable to a single module.

The question mark (?) is a special command. Entering the question mark following the prompt (B>) will return the Help menus as shown in Figure 5–3. These menus list all the system command words and a brief command description.

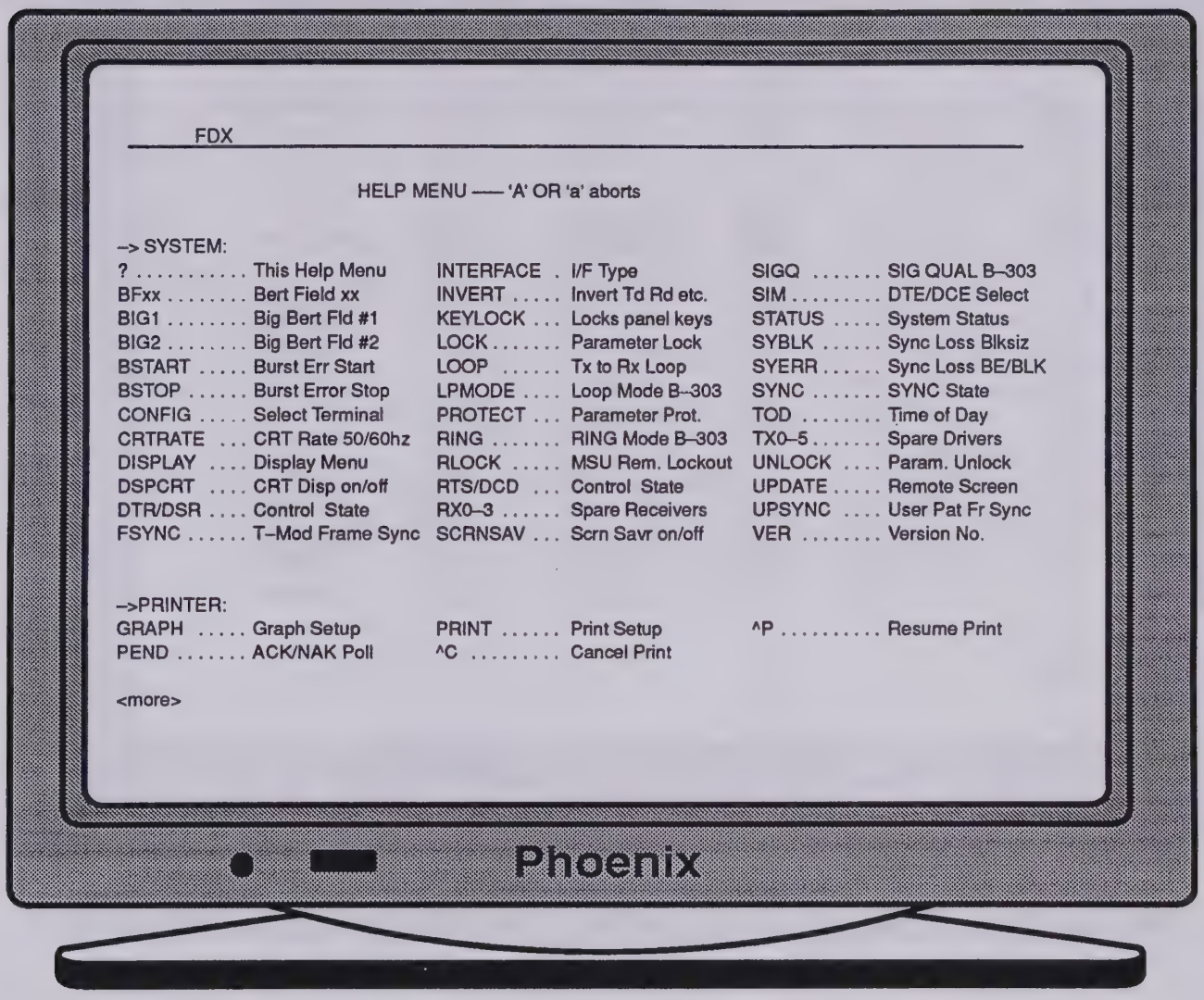
FDX
HELP MENU —— 'A' OR 'a' aborts
–> SYSTEM:
? ..... This Help Menu
BFxx ..... Bert Field xx
BIG1 ..... Big Bert Fld #1
BIG2 ..... Big Bert Fld #2
BSTART ..... Burst Err Start
BSTOP ..... Burst Error Stop
CONFIG ..... Select Terminal
CRTRATE ... CRT Rate 50/60hz
DISPLAY .... Display Menu
DSPCRT .... CRT Disp on/off
DTR/DSR .... Control State
FSYNC ..... T–Mod Frame Sync
INTERFACE . I/F Type
INVERT ..... Invert Td Rd etc.
KEYLOCK ... Locks panel keys
LOCK ..... Parameter Lock
LOOP ..... Tx to Rx Loop
LPMODE .... Loop Mode B–303
PROTECT ... Parameter Prot.
RING ..... RING Mode B–303
RLOCK ..... MSU Rem. Lockout
RTS/DCD ... Control State
RX0–3 ..... Spare Receivers
SCRNSAV ... Scrn Savr on/off
SIGQ ..... SIG QUAL B–303
SIM ..... DTE/DCE Select
STATUS ..... System Status
SYBLK ..... Sync Loss Blksiz
SYERR ..... Sync Loss BE/BLK
SYNC ..... SYNC State
TOD ..... Time of Day
TX0–5 ..... Spare Drivers
UNLOCK .... Param. Unlock
UPDATE ..... Remote Screen
UPSYNC .... User Pat Fr Sync
VER ..... Version No.
–>PRINTER:
GRAPH ..... Graph Setup
PEND ..... ACK/NAK Poll
PRINT ..... Print Setup
^C ..... Cancel Print
^P ..... Resume Print
<more>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 1.

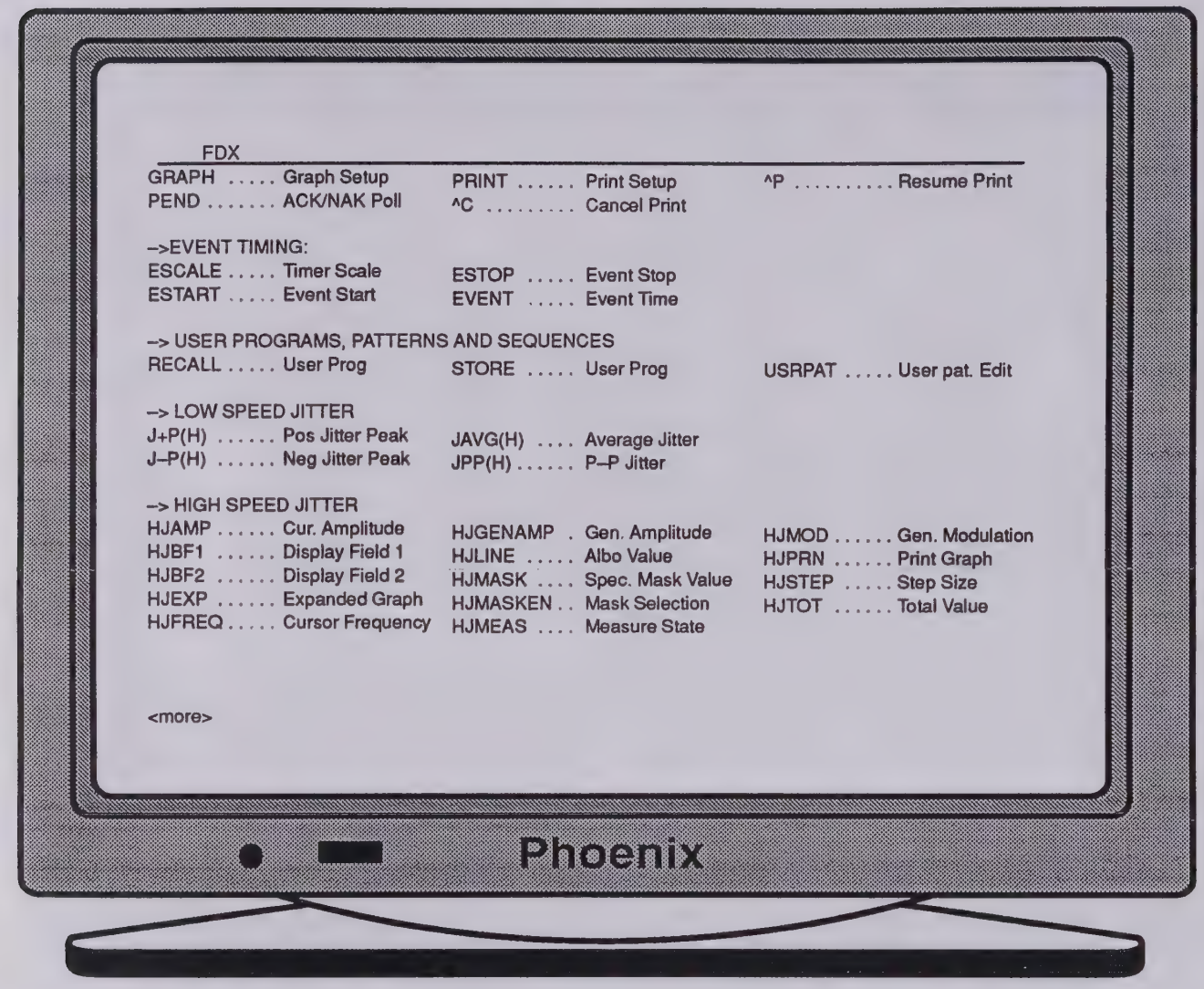
FDX
GRAPH ..... Graph Setup
PEND ..... ACK/NAK Poll
PRINT ..... Print Setup
^C ..... Cancel Print
^P ..... Resume Print
–>EVENT TIMING:
ESCALE ..... Timer Scale
ESTART ..... Event Start
ESTOP ..... Event Stop
EVENT ..... Event Time
–> USER PROGRAMS, PATTERNS AND SEQUENCES
RECALL ..... User Prog
STORE ..... User Prog
USRPAT ..... User pat. Edit
–> LOW SPEED JITTER
J+P(H) ..... Pos Jitter Peak
J–P(H) ..... Neg Jitter Peak
JAVG(H) .... Average Jitter
JPP(H) ..... P–P Jitter
–> HIGH SPEED JITTER
HJAMP ..... Cur. Amplitude
HJBF1 ..... Display Field 1
HJBF2 ..... Display Field 2
HJEXP ..... Expanded Graph
HJFREQ ..... Cursor Frequency
HJGENAMP . Gen. Amplitude
HJLINE ..... Albo Value
HJMASK .... Spec. Mask Value
HJMASKEN .. Mask Selection
HJMEAS .... Measure State
HJMOD ..... Gen. Modulation
HJPRN ..... Print Graph
HJSTEP ..... Step Size
HJTOT ..... Total Value
<more>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 2.

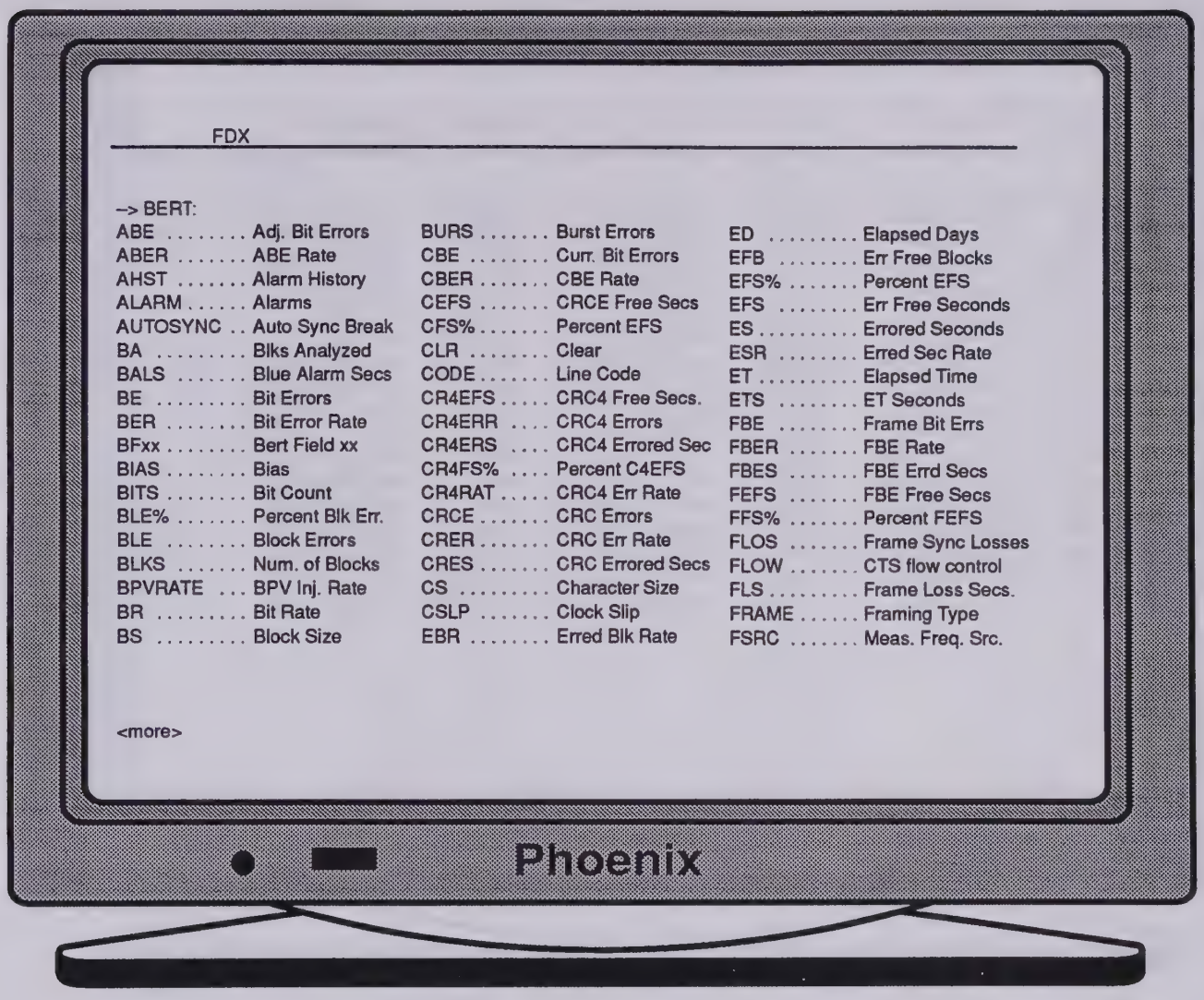
FDX
-> BERT:
ABE ..... Adj. Bit Errors
ABER ..... ABE Rate
AHST ..... Alarm History
ALARM ..... Alarms
AUTOSYNC .. Auto Sync Break
BA ..... Blks Analyzed
BALS ..... Blue Alarm Secs
BE ..... Bit Errors
BER ..... Bit Error Rate
BFxx ..... Bert Field xx
BIAS ..... Bias
BITS ..... Bit Count
BLE% ..... Percent Blk Err.
BLE ..... Block Errors
BLKS ..... Num. of Blocks
BPVRATE ... BPV Inj. Rate
BR ..... Bit Rate
BS ..... Block Size
BURS ..... Burst Errors
CBE ..... Curr. Bit Errors
CBER ..... CBE Rate
CEFS ..... CRCE Free Secs
CFS% ..... Percent EFS
CLR ..... Clear
CODE ..... Line Code
CR4EFS ..... CRC4 Free Secs.
CR4ERR .... CRC4 Errors
CR4ERS .... CRC4 Errored Sec
CR4FS% .... Percent C4EFS
CR4RAT ..... CRC4 Err Rate
CRCE ..... CRC Errors
CRER ..... CRC Err Rate
CRES ..... CRC Errored Secs
CS ..... Character Size
CSLP ..... Clock Slip
EBR ..... Erred Blk Rate
ED ..... Elapsed Days
EFB ..... Err Free Blocks
EFS% ..... Percent EFS
EFS ..... Err Free Seconds
ES ..... Errored Seconds
ESR ..... Erred Sec Rate
ET ..... Elapsed Time
ETS ..... ET Seconds
FBE ..... Frame Bit Errs
FBER ..... FBE Rate
FBES ..... FBE Errd Secs
FEFS ..... FBE Free Secs
FFS% ..... Percent FEFS
FLOS ..... Frame Sync Losses
FLOW ..... CTS flow control
FLS ..... Frame Loss Secs.
FRAME ..... Framing Type
FSRC ..... Meas. Freq. Src.
<more>
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Figure 5–3. Model 5500A Main Help Menu – Screen 3.

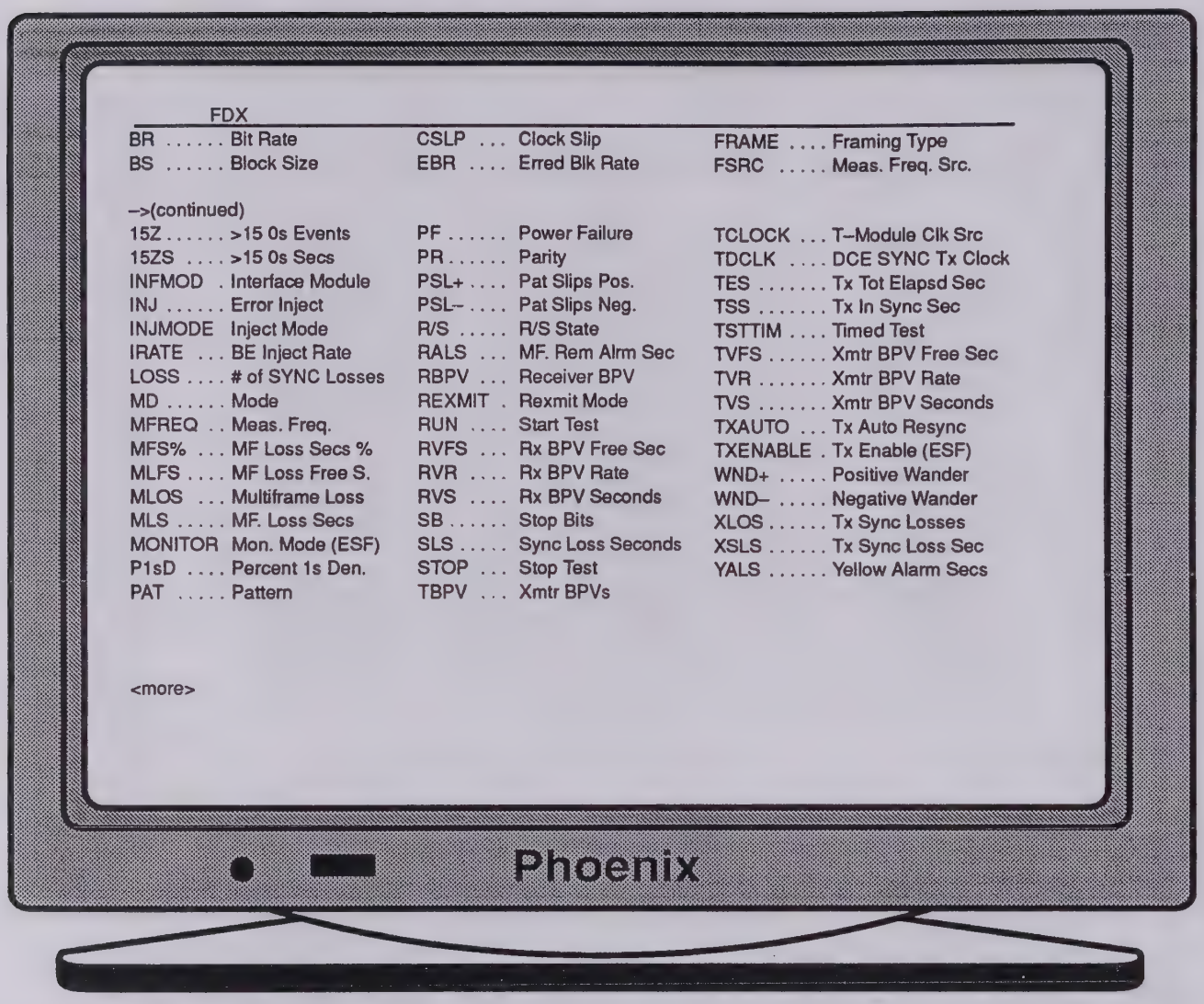
FDX
BR ..... Bit Rate
BS ..... Block Size
CSLP ... Clock Slip
EBR .... Erred Blk Rate
FRAME .... Framing Type
FSRC ..... Meas. Freq. Src.
–>(continued)
15Z ..... >15 0s Events
15ZS .... >15 0s Secs
INFMOD . Interface Module
INJ ..... Error Inject
INJMODE Inject Mode
IRATE ... BE Inject Rate
LOSS .... # of SYNC Losses
MD ..... Mode
MFREQ .. Meas. Freq.
MFS% ... MF Loss Secs %
MLFS .... MF Loss Free S.
MLOS ... Multiframe Loss
MLS ..... MF. Loss Secs
MONITOR Mon. Mode (ESF)
P1sD .... Percent 1s Den.
PAT ..... Pattern
PF ..... Power Failure
PR ..... Parity
PSL+ .... Pat Slips Pos.
PSL– .... Pat Slips Neg.
R/S ..... R/S State
RALS ... MF. Rem Alrm Sec
RBPV ... Receiver BPV
REXMIT . Rexmit Mode
RUN .... Start Test
RVFS ... Rx BPV Free Sec
RVR .... Rx BPV Rate
RVS .... Rx BPV Seconds
SB ..... Stop Bits
SLS ..... Sync Loss Seconds
STOP ... Stop Test
TBPV ... Xmtr BPVs
TCLOCK ... T–Module Clk Src
TDCLK .... DCE SYNC Tx Clock
TES ..... Tx Tot Elapsd Sec
TSS ..... Tx In Sync Sec
TSTTIM .... Timed Test
TVFS ..... Xmtr BPV Free Sec
TVR ..... Xmtr BPV Rate
TVS ..... Xmtr BPV Seconds
TXAUTO ... Tx Auto Resync
TXENABLE . Tx Enable (ESF)
WND+ ..... Positive Wander
WND– ..... Negative Wander
XLOS ..... Tx Sync Losses
XSLS ..... Tx Sync Loss Sec
YALS ..... Yellow Alarm Secs
<more>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 4.

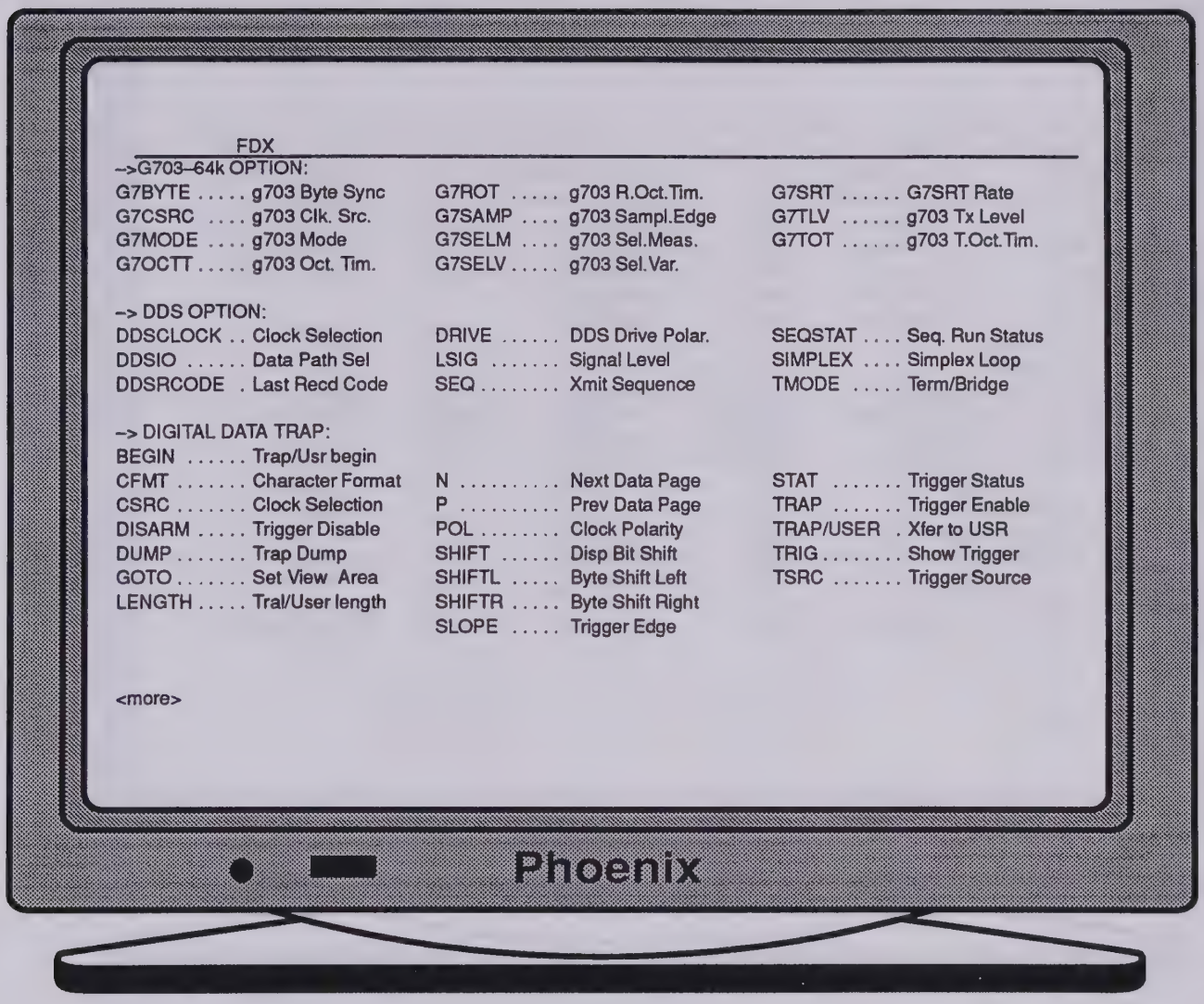
FDX
–>G703–64k OPTION:
G7BYTE ..... g703 Byte Sync
G7CSRC .... g703 Clk. Src.
G7MODE .... g703 Mode
G7OCTT ..... g703 Oct. Tim.
G7ROT ..... g703 R.Oct.Tim.
G7SAMP .... g703 Sampl.Edge
G7SELM .... g703 Sel.Meas.
G7SELV ..... g703 Sel.Var.
G7SRT ..... G7SRT Rate
G7TLV ..... g703 Tx Level
G7TOT ..... g703 T.Oct.Tim.
–> DDS OPTION:
DDSCLOCK .. Clock Selection
DDSIO ..... Data Path Sel
DDSRCODE . Last Recd Code
DRIVE ..... DDS Drive Polar.
LSIG ..... Signal Level
SEQ ..... Xmit Sequence
SEQSTAT .... Seq. Run Status
SIMPLEX .... Simplex Loop
TMODE ..... Term/Bridge
–> DIGITAL DATA TRAP:
BEGIN ..... Trap/Usr begin
CFMT ..... Character Format
CSRC ..... Clock Selection
DISARM ..... Trigger Disable
DUMP ..... Trap Dump
GOTO ..... Set View Area
LENGTH ..... Tral/User length
N ..... Next Data Page
P ..... Prev Data Page
POL ..... Clock Polarity
SHIFT ..... Disp Bit Shift
SHIFTL ..... Byte Shift Left
SHIFTR ..... Byte Shift Right
SLOPE ..... Trigger Edge
STAT ..... Trigger Status
TRAP ..... Trigger Enable
TRAP/USER . Xfer to USR
TRIG ..... Show Trigger
TSRC ..... Trigger Source
<more>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 5.

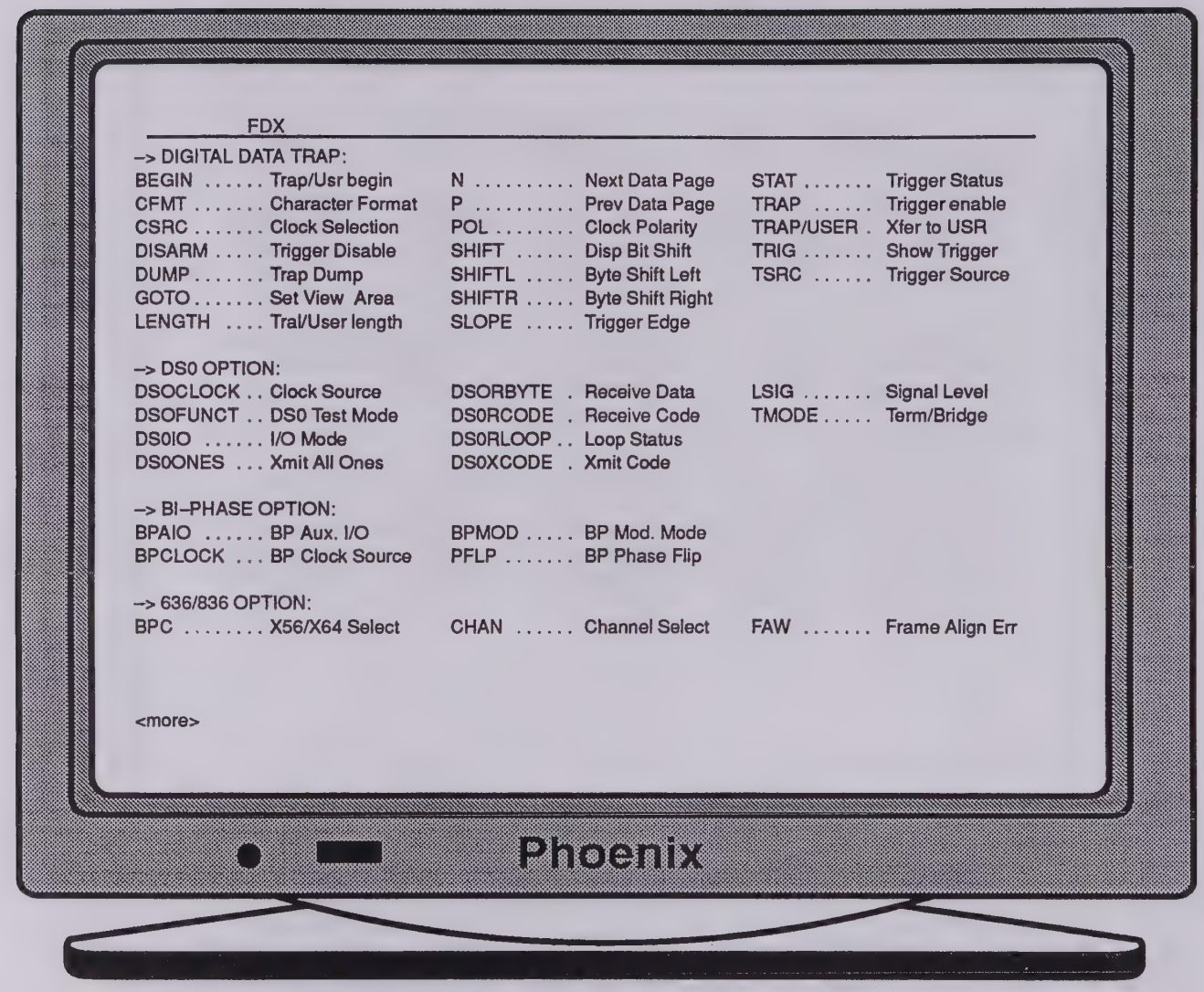
FDX
–> DIGITAL DATA TRAP:
BEGIN ..... Trap/Usr begin
CFMT ..... Character Format
CSRC ..... Clock Selection
DISARM ..... Trigger Disable
DUMP ..... Trap Dump
GOTO ..... Set View Area
LENGTH .... Tral/User length
N ..... Next Data Page
P ..... Prev Data Page
POL ..... Clock Polarity
SHIFT ..... Disp Bit Shift
SHIFTL ..... Byte Shift Left
SHIFTR ..... Byte Shift Right
SLOPE ..... Trigger Edge
STAT ..... Trigger Status
TRAP ..... Trigger enable
TRAP/USER . Xfer to USR
TRIG ..... Show Trigger
TSRC ..... Trigger Source
–> DS0 OPTION:
DSOCLOCK .. Clock Source
DSOFUNCT .. DS0 Test Mode
DS0IO ..... I/O Mode
DS0ONES ... Xmit All Ones
DSORBYTE . Receive Data
DS0RCODE . Receive Code
DS0RLOOP .. Loop Status
DS0XCODE . Xmit Code
LSIG ..... Signal Level
TMODE ..... Term/Bridge
–> BI–PHASE OPTION:
BPAIO ..... BP Aux. I/O
BPCLOCK ... BP Clock Source
BPMOD ..... BP Mod. Mode
PFLP ..... BP Phase Flip
–> 636/836 OPTION:
BPC ..... X56/X64 Select
CHAN ..... Channel Select
FAW ..... Frame Align Err
<more>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 6.

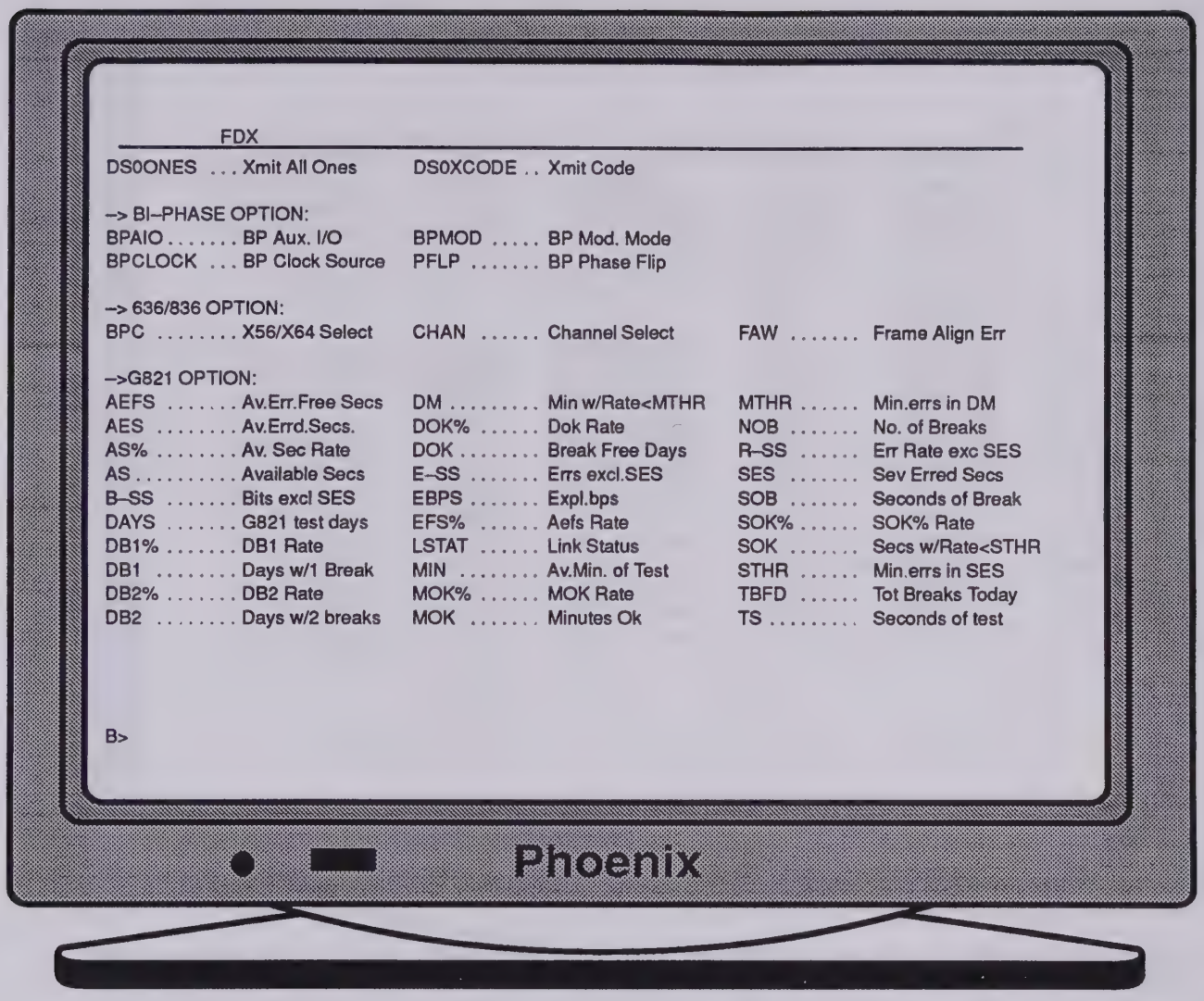
FDX
DS0ONES ... Xmit All Ones
DS0XCODE .. Xmit Code
–> BI–PHASE OPTION:
BPAIO ..... BP Aux. I/O
BPMOD ..... BP Mod. Mode
BPCLOCK ... BP Clock Source
PFLP ..... BP Phase Flip
–> 636/836 OPTION:
BPC ..... X56/X64 Select
CHAN ..... Channel Select
FAW ..... Frame Align Err
–>G821 OPTION:
AEFS ..... Av.Err.Free Secs
DM ..... Min w/Rate<MTHR
MTHR ..... Min.errs in DM
AES ..... Av.Errd.Secs.
DOK% ..... Dok Rate
NOB ..... No. of Breaks
AS% ..... Av. Sec Rate
DOK ..... Break Free Days
R–SS ..... Err Rate exc SES
AS ..... Available Secs
E–SS ..... Errs excl.SES
SES ..... Sev Erred Secs
B–SS ..... Bits excl SES
EBPS ..... Expl.bps
SOB ..... Seconds of Break
DAYS ..... G821 test days
EFS% ..... Aefs Rate
SOK% ..... SOK% Rate
DB1% ..... DB1 Rate
LSTAT ..... Link Status
SOK ..... Secs w/Rate<STHR
DB1 ..... Days w/1 Break
MIN ..... Av.Min. of Test
STHR ..... Min.errs in SES
DB2% ..... DB2 Rate
MOK% ..... MOK Rate
TBFD ..... Tot Breaks Today
DB2 ..... Days w/2 breaks
MOK ..... Minutes Ok
TS ..... Seconds of test
B>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 7.

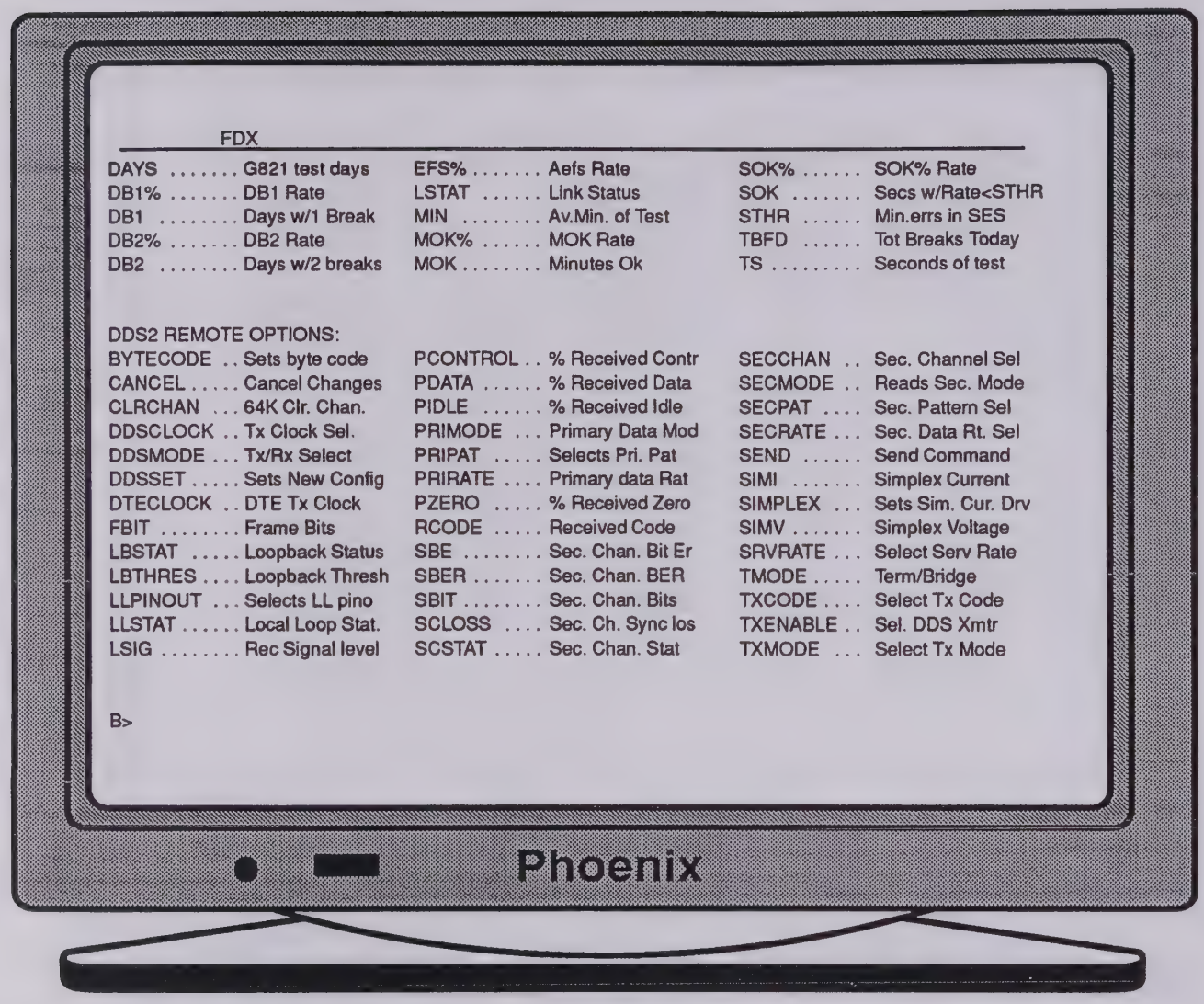
FDX
DAYS ..... G821 test days
DB1% ..... DB1 Rate
DB1 ..... Days w/1 Break
DB2% ..... DB2 Rate
DB2 ..... Days w/2 breaks
EFS% ..... Aefs Rate
LSTAT ..... Link Status
MIN ..... Av.Min. of Test
MOK% ..... MOK Rate
MOK ..... Minutes Ok
SOK% ..... SOK% Rate
SOK ..... Secs w/Rate<STHR
STHR ..... Min.errs in SES
TBFD ..... Tot Breaks Today
TS ..... Seconds of test
DDS2 REMOTE OPTIONS:
BYTECODE .. Sets byte code
CANCEL ..... Cancel Changes
CLRCHAN ... 64K Clr. Chan.
DDSCLOCK .. Tx Clock Sel.
DDSMODE ... Tx/Rx Select
DDSSET ..... Sets New Config
DTECLOCK .. DTE Tx Clock
FBIT ..... Frame Bits
LBSTAT ..... Loopback Status
LBTHRES .... Loopback Thresh
LLPINOUT ... Selects LL pino
LLSTAT ..... Local Loop Stat.
LSIG ..... Rec Signal level
PCONTROL .. % Received Contr
PDATA ..... % Received Data
PIDLE ..... % Received Idle
PRIMODE ... Primary Data Mod
PRIPAT ..... Selects Pri. Pat
PRIRATE .... Primary data Rat
PZERO ..... % Received Zero
RCODE ..... Received Code
SBE ..... Sec. Chan. Bit Er
SBER ..... Sec. Chan. BER
SBIT ..... Sec. Chan. Bits
SCLOSS .... Sec. Ch. Sync los
SCSTAT ..... Sec. Chan. Stat
SECCHAN .. Sec. Channel Sel
SECMODE .. Reads Sec. Mode
SECPAT .... Sec. Pattern Sel
SECRATE ... Sec. Data Rt. Sel
SEND ..... Send Command
SIMI ..... Simplex Current
SIMPLEX ... Sets Sim. Cur. Drv
SIMV ..... Simplex Voltage
SRVRATE ... Select Serv Rate
TMODE ..... Term/Bridge
TXCODE .... Select Tx Code
TXENABLE .. Sel. DDS Xmtr
TXMODE ... Select Tx Mode
B>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 8.

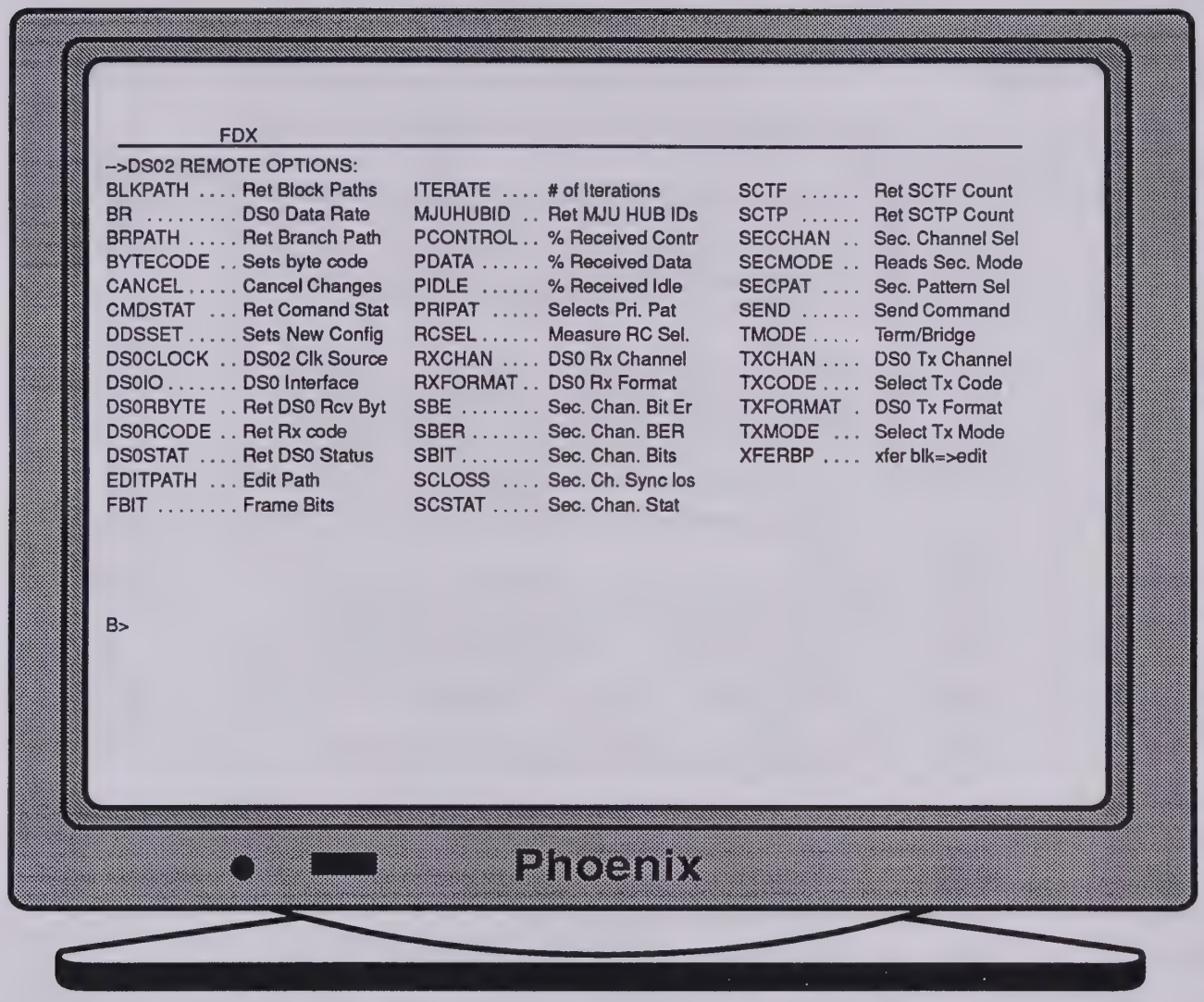
FDX
–>DS02 REMOTE OPTIONS:
BLKPATH .... Ret Block Paths
BR ..... DS0 Data Rate
BRPATH ..... Ret Branch Path
BYTECODE .. Sets byte code
CANCEL ..... Cancel Changes
CMDSTAT ... Ret Comand Stat
DDSSET ..... Sets New Config
DS0CLOCK .. DS02 Clk Source
DS0IO ..... DS0 Interface
DS0RBYTE .. Ret DS0 Rcv Byt
DS0RCODE .. Ret Rx code
DS0STAT .... Ret DS0 Status
EDITPATH ... Edit Path
FBIT ..... Frame Bits
ITERATE .... # of Iterations
MJUHUBID .. Ret MJU HUB IDs
PCONTROL .. % Received Contr
PDATA ..... % Received Data
PIDLE ..... % Received Idle
PRIPAT ..... Selects Pri. Pat
RCSEL ..... Measure RC Sel.
RXCHAN .... DS0 Rx Channel
RXFORMAT .. DS0 Rx Format
SBE ..... Sec. Chan. Bit Er
SBER ..... Sec. Chan. BER
SBIT ..... Sec. Chan. Bits
SCLOSS .... Sec. Ch. Sync los
SCSTAT ..... Sec. Chan. Stat
SCTF ..... Ret SCTF Count
SCTP ..... Ret SCTP Count
SECCHAN .. Sec. Channel Sel
SECMODE .. Reads Sec. Mode
SECPAT .... Sec. Pattern Sel
SEND ..... Send Command
TMODE ..... Term/Bridge
TXCHAN .... DS0 Tx Channel
TXCODE .... Select Tx Code
TXFORMAT . DS0 Tx Format
TXMODE ... Select Tx Mode
XFERBP .... xfer blk=>edit
B>
Phoenix

Figure 5–3. Model 5500A Main Help Menu – Screen 9.

5.4.1 System Commands

The system commands are configuration commands.
They are listed in Table 5–2.

Table 5–2. Model 5500A Remote System Commands

COMMAND	FUNCTION	INTERFACE
?	Returns screens as shown in Figure 5–2.	ALL
BFx	Returns the parameter displayed in the BERT RESULTS/ PARAM Menu field selected (where x = to number of field). Number of fields varies with installed interface module (i.e., with RS–232 x = 1 to 8).	ALL
BFx ?	Returns parameters that may be displayed in selected field. With RS–232 module, returns, "BITS, EMPTY, BE, BER, BLK, BLE, EFB, EBR, TOD, MDY, ET, ED, ETS, ES, EFS, ESR, LOS, SLS, PF, ABE, ABER, CBE, CBER, EFS%, PSL+, PSL–, BURS, BLE%, CODE, LSIG.	ALL
BFx XXXX	Sets selected field to display parameter entered from list above.	ALL
BIG(1,2)	Returns the parameter displayed in the selected BIG BERT Menu field selected (1 or 2).	ALL
BIG(1,2) ?	Returns parameters that may be displayed in selected field. With RS–232 module, returns, "BITS, EMPTY, BE, BER, BLK, BLE, EFB, EBR, TOD, MDY, ET, ED, ETS, ES, EFS, ESR, LOS, SLS, PF, ABE, ABER, CBE, CBER, EFS%, PSL+, PSL–, BURS, BLE%, CODE, LSIG.	ALL
BIG(1,2) XXXX	Sets selected field to display parameter entered from list above.	ALL
BSTART	Returns the burst error start threshold.	ALL
BSTART ?	Returns, "Burst error start threshold ... 1 to 15".	
BSTART xx	Sets burst error start threshold to desired level.	ALL
BSTOP	Returns the burst error stop threshold.	ALL
BSTOP ?	Returns, "Burst error stop threshold ... 1 to 50,000".	ALL
BSTOP xx	Sets burst error stop threshold to desired level.	ALL
CONFIG ?	Returns WYSE 50, TELEVIDEO 912/920, HAZELTINE 1500, FREEDOM 100, VT 100, ADM3A, VT 52, SUN, CUSTOM.	ALL
CONFIG		
CRTRATE ?	Returns, "50, 60".	ALL
CRTRATE xx	Sets 5500A CRT refresh rate to 50 or 60 Hz.	ALL
DISPLAY	Returns menu displayed on 5500A.	ALL
DISPLAY ?	Returns BERT, FORMAT, PROG, PAT, PRINT, CONFIG, GRAPH, REMOTE, BLACK, BIG, JITTER, MSU, G821, G–SELECT, TRAP, OPTMEN, DDSSEQ.	
DISPLAY xx	Changes menu displayed on 5500A to menu selected from list above.	ALL
DSPCRT	Returns status of the 5500A CRT display.	ALL
DSPCRT ?	Returns OFF, ON.	ALL
DSPCRT xx	Sets 5500A CRT display ON or OFF.	ALL
DTR/DSR	Returns state of DTR/DSR line.	LOW SPEED
DTR/DSR ?	Returns "Either "T" for TRUE or "F" for FALSE".	LOW SPEED
DTR/DSR xx	Sets state of DTR/DSR line to true or false.	LOW SPEED

Table 5–2. Model 5500A Remote System Commands(Cont.).

COMMAND	FUNCTION	INTERFACE
INTERFACE	Returns interface module installed in the 5500A.	ALL
INVERT	Returns status (inverted or normal) of listed parameters: TD RD TC RC XC.	ALL
INVERT ?	Returns "INVERT xxxxx .. where xxxxx is either "I" for invert or "." for noninvert, ordered TD,RD,TC,RC,XC".	ALL
INVERT xxxxx	Sets status of parameters as shown above.	ALL
KEYLOCK	Returns status of front panel keylock.	ALL
KEYLOCK ?	Returns, "DISABLE, ENABLE".	ALL
KEYLOCK xxxxx	Enables or disables 5500A front panel keys.	ALL
LOCK ?	Returns "ALL, RUN/STOP, INJECT, CLEAR, SYNC, RTS/DCD, DTR/DSR, DCE/DTE, RECALL, STORE, SELECT".	ALL
LOCK xx	Locks parameter entered from list above.	ALL
LOOP	Returns status of TX to RX loop.	ALL
LOOP ?	Returns "OFF, ON".	ALL
LOOP xx	Turns Tx to Rx loop on or off.	ALL
LPMODE	Returns status of loop mode.	Bell 303 only
LPMODE ?	Returns "SELFTEST, REMOTE".	Bell 303 only
LPMODE xx	Sets status of loop mode as above.	Bell 303 only
PROTECT	Sets protectable parameters to the protect state (This can be undone by using the UNLOCK ALL command described below.).	ALL
RING	Returns ring status.	Bell 303 only
RING ?	Returns "Correct Format ====>RING XXX, Where XXX is "ON" or "OFF"".	Bell 303 only
RING xxx	Sets ring to on or off.	Bell 303 only
RLOCK	Returns status of MSU remote lockout.	ALL
RLOCK ?	Returns "ENABLE, DISABLE".	ALL
RLOCK xx	Enables or disables MSU remote lockout.	ALL
RTS/DCD	Returns status of the RTS/DCD line.	
RTS/DCD ?	Returns "Either "T" for TRUE or "F" for FALSE".	
RTS/DCD x	Sets the RTS/DCD line true or false.	
RXn	Returns the status of the spare receiver lines where n=0, 1, 2, or 3.	ALL
SCRNSAV	Returns status of the 5500A screen saver.	ALL
SCRNSAV ?	Returns "DISABLE, ENABLE".	ALL
SCRNSAV xx	Enables or disables the screen saver.	ALL
SIGQ	Returns status of signal quality.	Bell 303 only
SIGQ ?	Returns "Correct Format ====>SIGQ XXX, Where XXX is "ON" or "OFF"".	Bell 303 only
SIGQ xxx	Turns signal quality on or off.	Bell 303 only
SIM	Returns status of DCE/DTE select.	Low Speed
SIM ?	Returns "DTE, DCE".	Low Speed

Table 5–2. Model 5500A Remote System Commands(Cont.).

COMMAND	FUNCTION	INTERFACE
SIM xx	Sets DCE/DTE select.	Low Speed
STATUS	Returns system status as "ROM: PASS, RAM: PASS, USER PROG: PASS, USER PAT: PASS".	ALL
SYBLK	Returns setting of sync loss criteria blocksize.	ALL
SYBLK ?	Returns, "Sync loss criteria (be/blk), enter blocksize ... 2 to 99,999".	ALL
SYBLK xxxxx	Sets sync loss criteria block size.	ALL
SYERR	Returns setting of sync loss criteria bit errors.	ALL
SYERR ?	Returns, "Sync loss criteria (be/blk), enter BE ... 1 to 50,000".	ALL
SYERR xxxxx	Sets sync loss criteria bit errors.	ALL
SYNC	Returns sync state.	ALL
SYNC ?	Returns Either "R" to reset sync loss or "B" to force sync break.	ALL
SYNC xx	Sets sync condition as above.	ALL
TOD	Returns setting of time of day, day of week, and month, date, year as "15:28:11.4 SU /3/16/87".	ALL
TOD ?	Returns "Time of Day Format: HH:MM:SS xx MM/DD/YY where xx = SU, MO, TU, WE, TH, FR, or SA".	ALL
TOD xx ...xx	Sets TOD in accordance with format above.	ALL
TXn	Returns state of spare transmit lines where n=0, 1, 2, 3, 4, or 5.	ALL
TXn ?	Returns "Either "T" for TRUE or "F" for FALSE" where n=0, 1, 2, 3, 4, or 5.	ALL
TXn xx	Sets state of spare transmit lines to true or false where n=0, 1, 2, 3, 4, or 5.	ALL
UNLOCK ?	Returns "ALL, RUN/STOP, INJECT, CLEAR, SYNC, RTS/DCD, DTR/DSR, DCE/DTE, RECALL, STORE, SELECT.	ALL
UNLOCK xx	Unlocks parameters selected from list above.	ALL
UPSYNC	Returns status of user pattern sync.	ALL
UPSYNC ?	Returns, "OFF, FRAME, MULTIFRAME".	ALL
UPSYNC xxxx	Sets status of user pattern sync per above.	
UPDATE	Brings the "Big Screen" display to the terminal (see NO TAG).	ALL
VER	Returns Model and version number as "PHOENIX 5500A, Vers. 7.06/7.06, Serial # 0"	ALL

5.4.2 Printer Commands

The printer commands are used to control the graph function of the 5500A and to control a printer connected to the 5500A. Two of these commands, <Control C> and <Control P> are direct action commands. They are used during the print and/or graph operation to exercise direct control over those functions. Entering <Control C> while the printer is printing will cause an interrupt and the printer will stop printing. Entering a <Control P> will remove the interrupt and the printer will return to its printing task.

Since the printer uses a small buffer, 256 bytes, there may be a discontinuity in the output print data when the printer has been interrupted and then restarted; however, the graph function is fully buffered and will not display any discontinuity if it is interrupted.

Another printer command is the PEND command. This command is used in the ACK – NACK mode to provide a

signal to the controller that the 5500A has something to output to the printer. The PEND command uses a 4–bit flag in the form:

PEND XXXX

For clarity, assigning a number to each position in the flag word gives:

PEND X3X2X1X0

This flag word is used by the 5500A to inform the controller if:

X0 = "1" that the 5500A has a data dump pending.

X1 = "1" that the 5500A has a data graph pending.

X2 = "1" that the 5500A has a jitter graph pending.

X3 = "1" that a key has been pushed on the 5500A that causes a one line printout to occur (ie., pressing error inject will cause the 5500A to output a single line output informing the user that the inject function is on or off).

The user may view the current PEND status by entering PEND which will return the flag word.

The user can force a bit in the flag word to a 1 by entering PEND XXXX with X = to 1 or 0. By setting one or more of the bits to a 1, a print dump of that function will be forced. At the completion of a print dump, either forced or controller selected, the controller will set the applicable bits back to zero.

The two remaining printer commands, GRAPH and PRINT involve multiple displays on the remote terminal. These commands will be explained and illustrated on the following pages.

The illustrations and examples on the following pages assume the user has an RS–232 interface module installed. If another interface module is installed in your unit, there may be differences in some of the displays. Normally these differences will appear on those displays that concern test parameters. For example, the graph data selection display, with the RS–232 interface, presents 12 parameters, but only those applicable to RS–232 may be graphed and/or printed. With the Framed T1 module installed, all the parameters on the same list may be graphed and/or printed. However, even though the number of parameters that may be graphed and/or printed has changed, the method of selecting the parameter to be graphed and/or printed remains the same.

To get to the print functions, the PRINT command is entered followed by a <RETURN>:

B>PRINT <RETURN>

The display will return:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: 1
```

To check the setting of the print enable/disable enter a "1" at the flashing cursor to change the display to:

```
Data printing is now: DISABLED
Enter 'C' to change or <RETURN> to exit: C
```

Entering a "C" will enable printing and change the display to:

```
Data printing is now: ENABLED
Enter 'C' to change or <RETURN> to exit: <RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: 2
```

Entering a 2 will bring up the print conditions and change the display to:

```
The available print conditions are:

(a)  1 MINUTE        (g)  6 HOUR        (m) TEST END
(b)  5 MINUTES       (h) 12 HOURS       (n) SYNC LOSS
(c) 1/ MINUTES       (i) 24 HOURS       (o) ERR SEC
(d) 15 MINUTES       (j) BIT ERROR      (p) ————————
(e) 3/ MINUTES       (k) BLOCK ERROR
(f)  1 HOUR          (l) BLOCK

The currently selected conditions are:

(1) 1/ MINUTES       (2) BLOCK
(3) ————————         (4) ————————

Enter number (1–4) and letter to select or <RETURN> to exit:3o
```

Entering "3o" will add errored seconds as a print condition and change the display to:

```
The available print conditions are:

(a)  1 MINUTE        (g)  6 HOUR        (m) TEST END
(b)  5 MINUTES       (h) 12 HOURS       (n) SYNC LOSS
(c) 1/ MINUTES       (i) 24 HOURS       (o) ERR SEC
(d) 15 MINUTES       (j) BIT ERROR      (p) ————————
(e) 3/ MINUTES       (k) BLOCK ERROR
(f)  1 HOUR          (l) BLOCK

The currently selected conditions are:

(1) 1/ MINUTES   (2) BLOCK
(3) ERR SEC      (4) ————————

Enter number (1–4) and letter to select or <RETURN> to exit:<RETURN>
```

Enter <RETURN> and the display returns to:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: 3
```

Enter a "3" to select data types to print and the display changes to:

```
(a)   BIT ERRORS –          (k)   FREQUENCY P
(b)   BIT ERROR RATE –      (l)   POWER LOSSES –
(c)   ELAPSED TIME P        (m)   ERRORED SECONDS P
(d)   ELAPSED TIME SECS –   (n)   ERROR FREE SECONDS –
(e)   BLOCK ERRORS P        (o)   ERRORED SECOND RATE –
(f)   ERRORED BLOCK RATE P, (p)   G821 –
(g)   BLOCKS –              (q)   JITTER FREE –
(h)   ERROR FREE BLOCKS –   (r)   JITTER HOLD –
(i)   SYNC LOSSES –         (s)   TIMER P
(j)   SYNC LOSS SECONDS P   (t)   BIAS P

"–" means don't print.  "P" means print.
Enter letter to change or <RETURN> to exit: g
```

Enter a "g" to add BLOCKS to the list of parameters to be printed and the display changes to:

```
(a)   BIT ERRORS –          (k)   FREQUENCY P
(b)   BIT ERROR RATE –      (l)   POWER LOSSES –
(c)   ELAPSED TIME P        (m)   ERRORED SECONDS P
(d)   ELAPSED TIME SECS –   (n)   ERROR FREE SECONDS –
(e)   BLOCK ERRORS P        (o)   ERRORED SECOND RATE –
(f)   ERRORED BLOCK RATE P  (p)   G821 –
(g)   BLOCKS P              (q)   JITTER FREE –
(h)   ERROR FREE BLOCKS –   (r)   JITTER HOLD –
(i)   SYNC LOSSES –         (s)   TIMER P
(j)   SYNC LOSS SECONDS P   (t)   BIAS P

"–" means don't print.  "P" means print.
Enter letter to change or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> and the display returns to:

```
1: Data print enable/disable
2: Select DATA print conditions
3: Select data types

Enter 1,2,3 or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> to get to the prompt and the prompt returns:

```
B>
```

To setup the graph conditions, enter the GRAPH command followed by a <RETURN>

B>GRAPH <RETURN>

The display appears as:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 1
```

To check graph enable/disable selection, enter a "1" at the flashing cursor to change the display to:

```
Graph printing is now: DISABLED
Enter 'C' to change or <RETURN> to exit: C
```

Enter a "C" to enable graph printing and change the display to:

```
Graph printing is now: ENABLED
Enter 'C' to change or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> to change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 2
```

Entering a "2" will allow the setting of the graph sample resolution and change the display to:

```
Graph sample resolution can be:

(1)  1 SECOND
(2) 10 SECONDS
(3)  1 MINUTE
(4) 10 MINUTES
(5)  1 HOUR

Current sample resolution is: 1 MINUTES
Enter number (1–5) to select or <RETURN> to exit: 3
```

Entering a "3" will select 1 minute for sample resolution and change the display to:

```
Graph sample resolution can be:

(1)  1 SECOND
(2) 10 SECONDS
(3)  1 MINUTE
(4) 10 MINUTES
(5)  1 HOUR

Current sample resolution is: 1 MINUTE
Enter number (1–5) to select or <RETURN> to exit:<RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 3
```

Entering a "3" permits selection of graph print resolution and changes the display to:

```
Graph print resolution can be:

(3)  1 MINUTE
(4) 10 MINUTES
(5)  1 HOUR

Current print resolution is: 1 MINUTE
Enter number (1–5) to select or <RETURN> to exit: 5
```

NOTE The print resolution is dependent upon the sample resolution. The print resolution can never be greater than the sample resolution nor can it be more than 2 steps less. Therefore the print resolution display will adjust itself to permit the user to select only the valid print resolution scale dependent upon the setting of the sample resolution.

Entering a "5" will select 1 hour for print resolution and change the display to:

```
Graph print resolution can be:

(3)  1 MINUTE
(4) 10 MINUTES
(5)  1 HOUR

Current print resolution is: 1 HOUR
Enter number (1–5) to select or <RETURN> to exit: <RETURN>
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: 4
```

Entering a "4" permits selection of graph data and changes the display to:

```
(a)  BIT ERRORS —                  (g)  > 15 ZEROS —
(b)  ERRORED SECONDS G–            (h)  SEVERELY ERRORED SECS GP
(c)  FRAME BIT ERRORS G–           (i)  WANDER POSITIVE —
(d)  F–BIT ERRORED SECONDS GP      (j)  WANDER NEGATIVE —
(e)  CRC ERR / MF LOSSES G–        (k)  SYNC LOSSES —
(f)  FRAME LOSSES —                (l)  RECEIVE BPV'S

"G–" means graph only, "GP" means graph and print.
Enter letter (a–l) to change or <RETURN> to exit: c
```

Entering a "b" will change errored seconds from graph only to graph and print while the display changes to:

```
(a)  BIT ERRORS —                  (g)  > 15 ZEROS —
(b)  ERRORED SECONDS GP            (h)  SEVERELY ERRORED SECS GP
(c)  FRAME BIT ERRORS G–           (i)  WANDER POSITIVE —
(d)  F–BIT ERRORED SECONDS GP      (j)  WANDER NEGATIVE —
(e)  CRC ERR / MF LOSSES G–        (k)  SYNC LOSSES —
(f)  FRAME LOSSES —                (l)  RECEIVE BPV'S

"G–" means graph only, "GP" means graph and print.
Enter letter (a–l) to change or <RETURN> to exit: c
```

Entering a <RETURN> will change the display to:

```
1: Graph print enable/disable
2: Select graph SAMPLE resolution
3: Select graph PRINT resolution
4: Select graph data

Enter 1,2,3,4 or <RETURN> to exit: <RETURN>
```

Enter a <RETURN> and the prompt returns:

```
B>
```

5.4.3 Event Timing Commands

The event timing commands permit the user to set a timer to record the time between selected intervals. The event timing commands are presented Table 5–3.

Table 5–3. Model 5500A Remote Event Timing Commands.

COMMAND	FUNCTION	INTERFACE
ESCALE	Returns scale that the ESTART to ESTOP is measured in.	Low Speed
ESCALE ?	Returns "1S, 10S, .1MS, 1MS, 10MS"	Low Speed
ESCALE xx	Sets timer scale to one of the above listed intervals.	Low Speed
ESTART	Returns the event that will start the timer.	Low Speed
ESTART ?	Returns "RD/, RD\, TD/, TD\, SQ/, SQ\, DTR/, DTR\, DCD/, DCD\, DSR/, DSR\, CTS/, CTS\, RTS/, RTS\". (LTMD)	Low Speed
ESTART xxx	Sets the event to start the timer from the above list.	Low Speed
ESTOP	Returns the event that will stop the timer.	Low Speed
ESTOP ?	Returns "RD/, RD\, TD/, TD\, SQ/, SQ\, DTR/, DTR\, DCD/, DCD\, DSR/, DSR\, CTS/, CTS\, RTS/, RTS\, SNGL, CONT, OFF".	Low Speed
ESTOP xxx	Selects the event to stop the timer from the above list.	Low Speed
EVENT	Returns the time between the start and stop events selected by ESTART and ESTOP above. The event time measurement is returned in the units selected by ESCALE above with a maximum resolution of 1 ns. If the event has not occurred, the response will be "–". If the event exceeds the counter range (4.75 seconds) the response will be OVER. If more than 10 seconds have elapsed since the last event time measurement was made, the response will have an "I" appended to it indicating inactivity.	Low Speed

5.4.4 User Programs, Patterns, and Sequence Commands

The user program, pattern, and sequence commands are used to create and store programs and patterns in memory for future use. Table 5–4 presents the user programs and patterns commands. The sequence command (SEQ) is used with the DDS Bell 303 module only and is explained in the Bell 303 option section of this manual.

Table 5–4. Model 5500A Remote User Programs and Patterns Commands.

COMMAND	FUNCTION	INTERFACE
RECALL	Returns locations and names of all previously stored programs.	ALL
RECALL ?	Returns "Select program 0–9".	ALL
RECALL x	Recalls the program number as selected by 'x'.	ALL
STORE	Returns locations and names of all previously stored programs.	ALL
STORE ?	Returns "Form: STORE # '———name ———' where: # = 0–9".	ALL
STORE x'name'	Stores the current program setup in the location specified and with the name assigned.	ALL
USRPAT	Returns the current remote selected user pattern for editing.	ALL
USRPAT = x	Selects user pattern 1, 2, 3, or 4.	ALL
USRPAT ?	Returns "Enter HEX data separated by spaces. Enter '+' before the data to add it the present pattern. Otherwise, the old pattern is replaced by the new data. Enter '=' followed by 1–4 to change pattern number."	ALL
USRPAT + xx...xx	Adds HEX value of xx to current pattern.	ALL
USRPAT xx ... xx	Replaces current pattern with one defined by HEX values of xx.	ALL

5.4.5 Digital Data Trap Commands

The digital data trap commands are used to configure the digital data trap from a remote terminal. The commands are presented in Table 5–5.

Table 5–5. Model 5500A Remote Digital Data Trap Commands.

COMMAND	FUNCTION	INTERFACE
BEGIN	Returns beginning location of that portion of the data trapped in the trap buffer that is to be stored into user pattern number 4.	ALL
BEGIN ?	Returns "Set begin location from 0 to 63999".	ALL
BEGIN xxxx	Sets begin point to value expressed in xxxx.	ALL
CFMT	Returns character format of trapped data.	ALL
CFMT ?	Returns "BIN, HXM, HXL"	ALL
CFMT xxx	Sets character format as listed above.	ALL
CSRC	Returns default setting (RC) of the trigger clock selection. Future software enhancements may permit selection of trigger clock selection.	ALL
DISARM	Disables the trigger if the trap has tripped due to a BE.	ALL
DUMP	Dumps the contents of the trap buffer to the remote terminal or printer.	ALL
GOTO	Returns current cursor location.	ALL
GOTO ?	Returns "Set go to location from 0 to 63999"	ALL
GOTO xxxxx	Sets cursor to location specified by xxxx.	ALL
N	Scrolls remote display to next page in trap buffer.	ALL
P	Scrolls remote display to previous page in trap buffer.	ALL
POL	Returns default setting (N) of the trigger polarity. Future software enhancements may permit selection of trigger polarity.	ALL
SHIFT	Displays the current relative shift in the data bits being viewed.	ALL
SHIFTL	Shifts the relative view one bit to the left.	ALL
SHIFTR	Shifts the relative view one bit to the right.	ALL
SLOPE	Returns default setting (+) of the trigger slope. Future software enhancements may permit selection of trigger slope.	ALL
STAT	Returns status of the trigger (triggered/stopped or armed).	ALL
TRAP	Enables the trigger.	ALL
TRAP/USER	Transfers the selected bits in the trap buffer into user pattern number four.	ALL
TRIG	Returns current trigger position setting.	ALL
TRIG ?	Returns "MID, POST, PRE"	ALL
TRIG xxx	Sets trigger location to one of the above positions.	ALL
TSRC	Returns default setting (BE) of the trigger source. Future software enhancements may permit selection of trigger source.	ALL

5.4.6 BERT Setup Commands

The BERT setup commands are used to configure the 5500A for a particular user application. These commands are normally entered with a parameter. Table 5–6 presents the BERT setup commands.

Table 5–6. Model 5500A Remote BERT Setup Commands.

COMMAND	FUNCTION	INTERFACE
AUTOSYNC	Returns current status of auto resync function.	ALL
AUTOSYNC ?	Returns "Forms: Autosync Disable Autosync Enable Autosync Timed XXX ===> where XXX equals numbers from 0–999 x 10 milliseconds."	ALL
AUTOSYNC xx	Sets auto sync function per above format.	ALL
BLKS	Returns the number of blocks that will be analyzed for this test.	ALL
BLKS ?	Returns "Number of blocks to analyze from 0 to 9999, 0 = continuous."	ALL
BLKS xx	Sets number of blocks to be analyzed as selected by xx.	ALL
BPVRATE	Returns the current bipolar violation error injection rate.	T1/T1C
BPVRATE ?	Returns "The injected BPV rate is programmable in the form: mE–e where: m= 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 e = 3, 4, 5, 6, 7".	T1/T1C
BPVRATE mE–e	Sets the BPV inject rate per the above.	T1/T1C
BR	Returns current bit rate.	ALL
BR ?	Returns "COMMAND DESCRIPTION: BR RETURNS PRESENT BIT RATE SELECTION BR ? FOR HELP THE FOLLOWING PARAMETERS ARE THE CHOICES FOR THIS MODULE OR A NON STANDARD BIT RATE MAY BE CHOSEN. 1.544M".	ALL
BR xx	Sets bit rate to value selected by xx as above.	ALL
BS	Returns current block size.	ALL
BS ?	Returns "10^2, 10^3, 10^4, 10^5, 10^6, 10^7,10^8, 10^9".	ALL
BS 10^x	Sets block size to selected value per x where x = 2, 3, 4, 5, 6, 7, 8, or 9.	ALL
CLR	This command clears all registers and sets them to zero.	ALL
CODE	Returns line code setting.	T1/T1C
CODE ?	Returns "AMI, B8ZS" "AMI, HDB3", or "B8ZS, HDB3".	T1/G.703
CODE xx	Sets line code to selected code.	T1/G.703
CS	Returns current character size.	Low Speed
CS ?	Returns "5, 6, 7, 8, CONT".	Low Speed
CS xx	Sets character size to one of above.	Low Speed
FLOW	Returns state of CTS flow control.	Low Speed
FLOW ?	Returns "OFF, CTS".	Low Speed
FLOW xxx	Sets state of CTS FLOW.	Low Speed
FRAME	Returns current frame state.	T1 (628/636)

Table 5–6. Model 5500A Remote BERT Setup Commands.(Cont.)

COMMAND	FUNCTION	INTERFACE
FRAME ?	Returns "DISABLE, D4, ESF, SLC96".	T1 (628/636)
FRAME XX	Disables or sets framing.	T1 (628/636)
FSRC	Returns parameter being measured by frequency counter.	ALL
FSRC ?	Returns "BR, TC, RC, XC".	ALL
FSRC xx	Selects parameter to be measured by frequency counter.	ALL
INJ	Returns status of error injection.	ALL
INJ ?	Returns "OFF, ON".	ALL
INJ xx	Turns error injection on or off.	ALL
INJMODE	Returns injection mode status.	628/636/828 /836/815
INJMODE ?	Returns "BPV, F–BIT, DATA, CRC".	628/636/828 /836/815
INJMODE xx	Sets the injection mode to desired status.	628/636/828 /836/815
IRATE	Returns the injected error rate.	ALL
IRATE ?	Returns "The injected error rate is programmable in the form: mE–e where: m= 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 e = 2, 3, 4, 5, 6, 7, 8, 9".	ALL
IRATE mE–e	Sets the error inject rate per the above.	ALL
MD	Returns current mode.	ALL
MD ?	Returns "ASYNC, SYNC or BRIDGE, TERM".	ALL
MD xx	Sets mode per above.	
MONITOR	Returns status of MONITOR mode.	628/636
MONITOR ?	Returns "ENABLE, DISABLE".	628/636
MONITOR xx	Enables or disables monitor mode.	628/636
PAT	Returns current transmit pattern.	ALL
PAT ?	Returns "63, 511, 2047, REV2047, (2^15)–1, (2^20)–1, QRW, LOOP–UP, LOOP–DN, MARK, SPACE, ALT, FOX, FOX2, SYSY–511, X25–511, (2^9)–1A, NET55, 1:7, 3:24, USR1, USR2, USR3, USR4"	ALL
PAT xx	Sets transmit pattern to one of above.	ALL
PR	Returns async parity setting.	Low Speed
PR ?	Returns "NONE, EVEN, ODD".	Low Speed
PR xx	Sets async parity as above.	Low Speed
REXMIT	Returns the status of the retransmit mode.	G.703
REXMIT ?	Returns "On, Off".	G.703
REXMIT xx	Turns retransmit mode on or off.	G.703
RUN	Starts test.	ALL
SB	Returns number of stop bits.	Low Speed
SB ?	Returns "1, 2".	Low Speed

Table 5–6. Model 5500A Remote BERT Setup Commands.(Cont.)

COMMAND	FUNCTION	INTERFACE
SB x	Sets number of stop bits to 1 or 2.	Low Speed
SEQ	Returns DDS sequence.	DDS
SEQ ?	Returns "Form : SEQ x x x Rx where R = repeat, and x = hex digit or: ZS, OS, OF, ID, PAT, RPAT, RZ6, ROS, RLB, ROF, RID".	DDS
SEQ xx	Sets the sequence to that selected.	DDS
STOP	Stops test.	ALL
TCLOCK	Returns the clock source for the T1 clock being used.	ALL T
TCLOCK ?	Returns "RX, INTERNAL, EXTERNAL, USER, THRU, JITTER, THRU+JIT, THRU–JIT".	ALL T
TCLOCK xxx	Sets clock source to selection made from above list.	ALL T
TDCLK	Returns clock that is used as DCE mode transmit clocking signal.	Low Speed
TDCLK ?	Returns "TC, XC".	Low Speed
TDCLK xx	Selects DCE mode transmit clocking signal.	Low Speed
TXAUTO	Returns transmit auto resync status.	815
TSTTIM	Returns length of timed test.	ALL
TSTTIM ?	Returns "Enter test time as HH:MM:SS	ALL
TSTTIM xx:xx:xx	Sets test time per format above.	ALL
TXAUTO ?	Returns "ENABLE, DISABLE".	815
TXAUTO xx	Enables or disables transmit auto resync.	815
TXENABLE	Returns status of transmitter in BRIDGE or MONITOR mode.	628/636/828/836
TXENABLE ?	Returns "ON, OFF".	628/636/828/836
TXENABLE xx	Turns transmitter on or off in BRIDGE or MONITOR.	628/636/828/836

5.4.7 BERT Result Commands

The BERT results commands are used to monitor the results of particular BERT functions. In most cases these commands are direct entry commands that do not support a parameter. The exceptions to this will be noted in Table 5–7 which lists the BERT results commands.

Table 5–7. Model 5500A Remote BERT Results Commands.

COMMAND	FUNCTION	INTERFACE
ABE	Returns adjusted bit errors.	ALL
ABER	Returns adjusted bit error rate.	ALL
AHST	Returns alarm history.	T1/T1C
ALARM	Returns alarms status.	T1/T1C
BA	Returns number of blocks analyzed.	ALL
BALS	Returns number of blue alarm seconds.	628/636/828/836
BE	Returns number of bit errors.	ALL
BER	Returns the bit error rate.	ALL
BIAS	Returns the bias measurement.	Low Speed
BITS	Returns current bit count.	ALL
BLE%	Returns percent of errored blocks.	ALL
BLE	Returns number of block errors.	ALL
BURS	Returns number of burst errors.	ALL
CBE	Returns number of current bit errors.	ALL
CBER	Returns current bit error rate.	ALL
CEFS	Returns CRC error free seconds.	628/636
CFS%	Returns percent of CRC error free seconds.	628/636
CR4EFS	Returns CRC4 error free seconds.	G.703
CR4ERR	Returns CRC4 errors.	G.703
CR4ERS	Returns CRC4 errored seconds.	G.703
CR4FS%	Returns percent of CRC4 error free seconds.	G.703
CR4RAT	Returns the CRC4 error rate.	G.703
CRCE	Returns number of CRC errors.	628/636
CRER	Returns CRC error rate.	628/636
CRES	Returns CRC errored seconds.	628/636
CSLP	Returns clock slip.	628/636/828/836
EBR	Returns errored block rate.	ALL
ED	Returns number of elapsed days since test began.	ALL
EFB	Returns the number of error free blocks.	ALL
EFS%	Returns percent of error free seconds.	ALL
EFS	Returns number of error free seconds.	ALL
ES	Returns number of errored seconds.	ALL
ESR	Returns the errored second rate.	ALL
ET	Returns elapsed time since test began.	ALL
ETS	Returns elapsed time in seconds since test began.	ALL

Table 5–7. Model 5500A Remote BERT Results Commands.(Cont.)

COMMAND	FUNCTION	INTERFACE
FBE	Returns frame bit errors.	628/636/828/836
FBER	Returns frame bit error rate.	628/636/828/836
FBES	Returns frame bit errored seconds.	628/636/828/836
FEFS	Returns frame bit error free seconds.	628/636/828/836
FFS%	Returns percent of frame bit error free seconds.	628/636/828/836
FLOS	Returns frame sync losses.	628/636/828/836
FLS	Returns number of frame loss seconds.	628/636/828/836
15Z	Returns # of 15 zeros events.	628/636/828/836
15ZS	Returns 15 zeros seconds.	628/636/828/836
LOSS	Returns number of sync losses.	ALL
MFREQ	Returns frequency of selected data stream	ALL
MFS%	Returns percent of multiframe loss seconds.	828/836
MLFS	Returns multiframe loss free seconds.	828/836
MLOS	Returns multiframe loss of sync (count).	828/836
MLS	Returns loss seconds.	828/836
P1sD	Returns percent of one's density.	ALL T
PSL+	Returns positive pattern sync losses.	ALL
PSL–	Returns negative pattern sync losses.	ALL
R/S	Returns run/stop status.	ALL
RALS	Returns multiframe remote alarm seconds.	828/836
RBPV	Returns receiver bipolar violations.	T1/G.703
RVFS	Returns receiver BPV seconds.	T1/G.703
RVR	Returns receiver BPV rate.	T1/G.703
RVS	Returns receiver BPV seconds.	T1/G.703
SLS	Returns sync loss seconds.	ALL
TBPV	Returns transmit bipolar violations.	600
TES	Returns transmit total elapsed seconds.	815
TSS	Returns transmit in–sync seconds	815
TVFS	Returns transmit BPV free seconds.	600
TVR	Returns transmit BPV rate.	600
TVS	Returns transmit BPV seconds.	600
WND+	Returns wander positive.	628/636/828/836
WND–	Returns wander negative.	628/636/828/836
XLOS	Returns transmit sync losses.	815
XSLS	Returns transmit sync loss seconds.	815
YALS	Returns yellow alarm seconds.	628/636

5.4.8 Low Speed Jitter

There are four remote commands associated with the low speed jitter function. The commands are:

J+P(H) – returns positive peak jitter

J–P(H) – returns negative peak jitter

JAVG(H) – returns average jitter

JPP(H) – returns peak–to–peak jitter

The "(H)" is an optional parameter. When the (H) is included, it returns the highest peak value of that parameter during the test time. If the (H) is omitted, the value at the present time is returned.

5.4.9 Module Remote Commands

There are other remote commands that are specific to a particular interface module (ie., the high speed jitter commands). These commands are discussed in the instruction manual for the specific interface module.

The G.821 remote commands are discussed in section 6 of this manual.

5.5 REMOTE "BIG SCREEN" DISPLAY

To configure the terminal for the "Big Screen" display, type <CONFIG?>. Select the setting closest to the terminal type. The "BIG SCREEN" display, presented in Figure 5–4, provides the user with a current display of all the test parameters. This four page display (brought to the screen by the UPDATE command) is continually updated. The user may "freeze" the display by pressing the <1> key. While this freezes the current display, it does not stop the accumulation of data. The display will update as soon as the freeze command is removed (by pressing the <1> key). Additionally, through the use of the designated keys, Run/Stop <2>, Clear <3>, Error Injection <4>, and Sync <5> may be controlled from this display. The <P> key permits the user to scroll through the four page display and the <Q> key will return the user to the system prompt "B>".

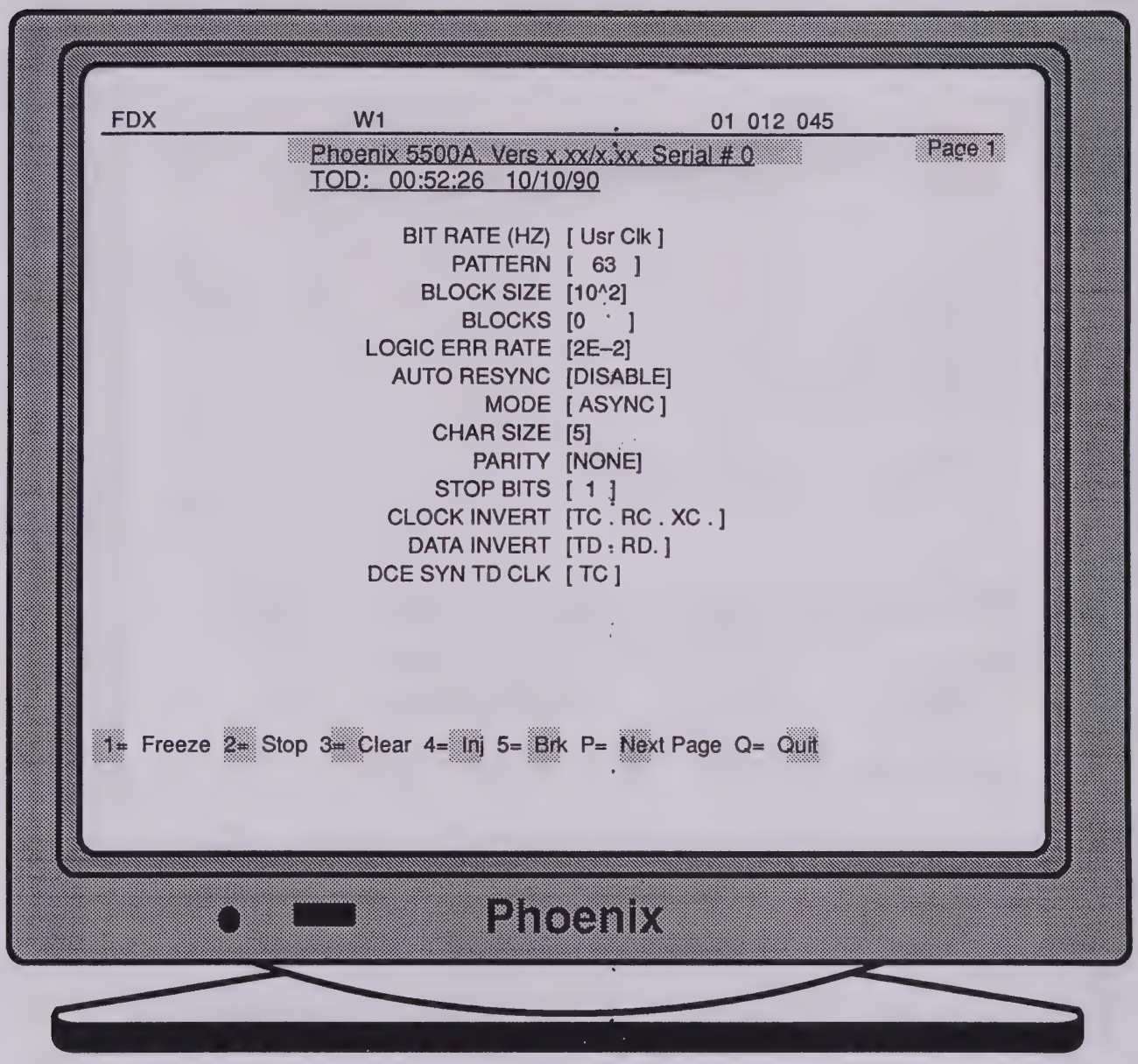
FDX W1 01 012 045
Phoenix 5500A Vers x.xx/x.xx Serial # 0
Page 1
TOD: 00:52:26 10/10/90
BIT RATE (HZ) [Usr Clk]
PATTERN [63]
BLOCK SIZE [10^2]
BLOCKS [0]
LOGIC ERR RATE [2E–2]
AUTO RESYNC [DISABLE]
MODE [ASYNC]
CHAR SIZE [5]
PARITY [NONE]
STOP BITS [1]
CLOCK INVERT [TC . RC . XC .]
DATA INVERT [TD . RD.]
DCE SYN TD CLK [TC]
1= Freeze 2= Stop 3= Clear 4= Inj 5= Brk P= Next Page Q= Quit
Phoenix

Figure 5–4. 5500A Remote "Big Screen" Display – Page 1.

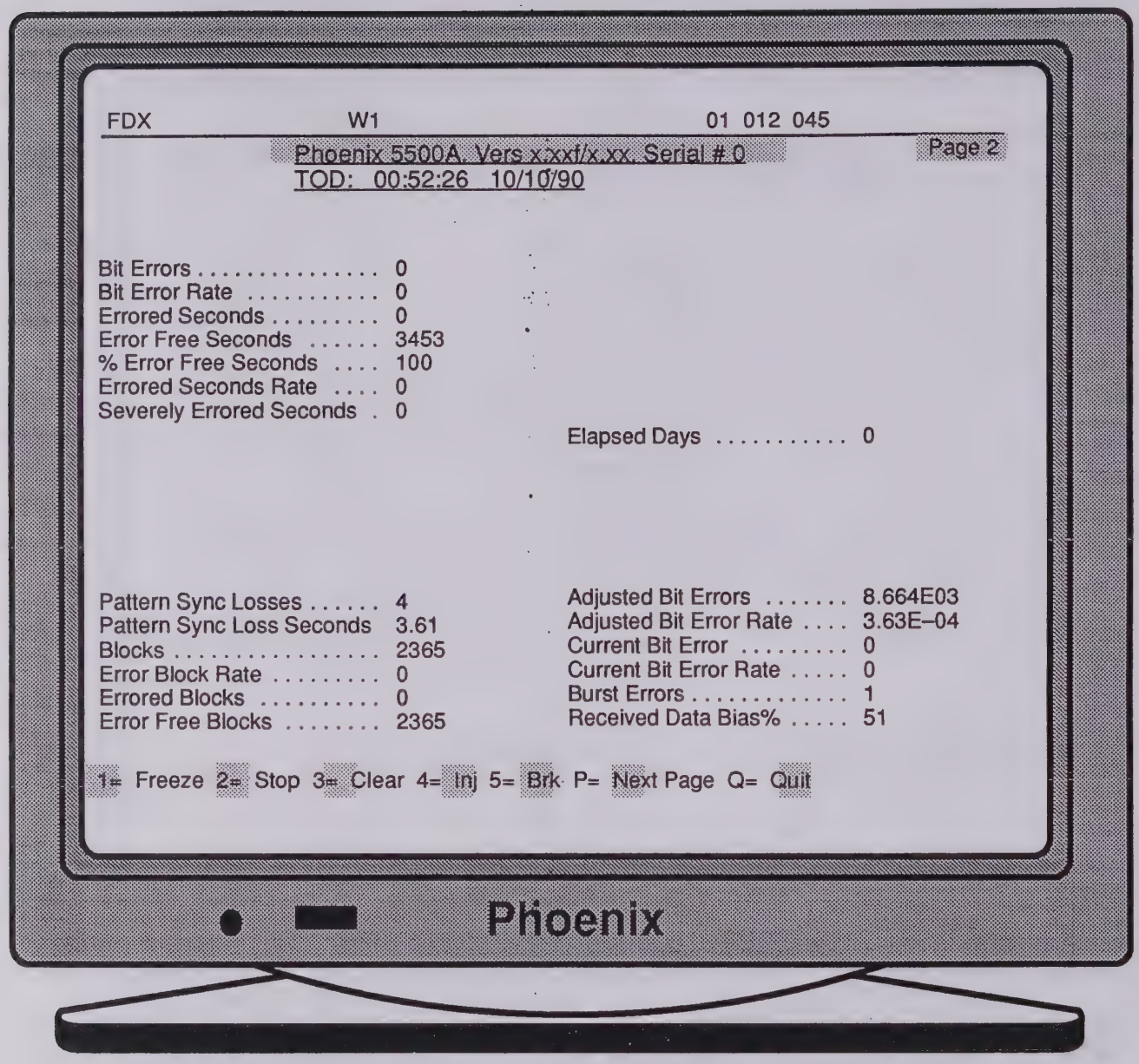
FDX W1 01 012 045
Phoenix 5500A Vers x.xxf/x.xx Serial # 0
Page 2
TOD: 00:52:26 10/10/90
Bit Errors 0
Bit Error Rate 0
Errored Seconds 0
Error Free Seconds 3453
% Error Free Seconds 100
Errored Seconds Rate 0
Severely Errored Seconds . 0
Elapsed Days 0
Pattern Sync Losses 4
Pattern Sync Loss Seconds 3.61
Blocks 2365
Error Block Rate 0
Errored Blocks 0
Error Free Blocks 2365
Adjusted Bit Errors 8.664E03
Adjusted Bit Error Rate 3.63E–04
Current Bit Error 0
Current Bit Error Rate 0
Burst Errors 1
Received Data Bias% 51
1= Freeze 2= Stop 3= Clear 4= Inj 5= Brk P= Next Page Q= Quit
Phoenix

Figure 5–4. 5500A Remote "Big Screen" Display – Page 2.

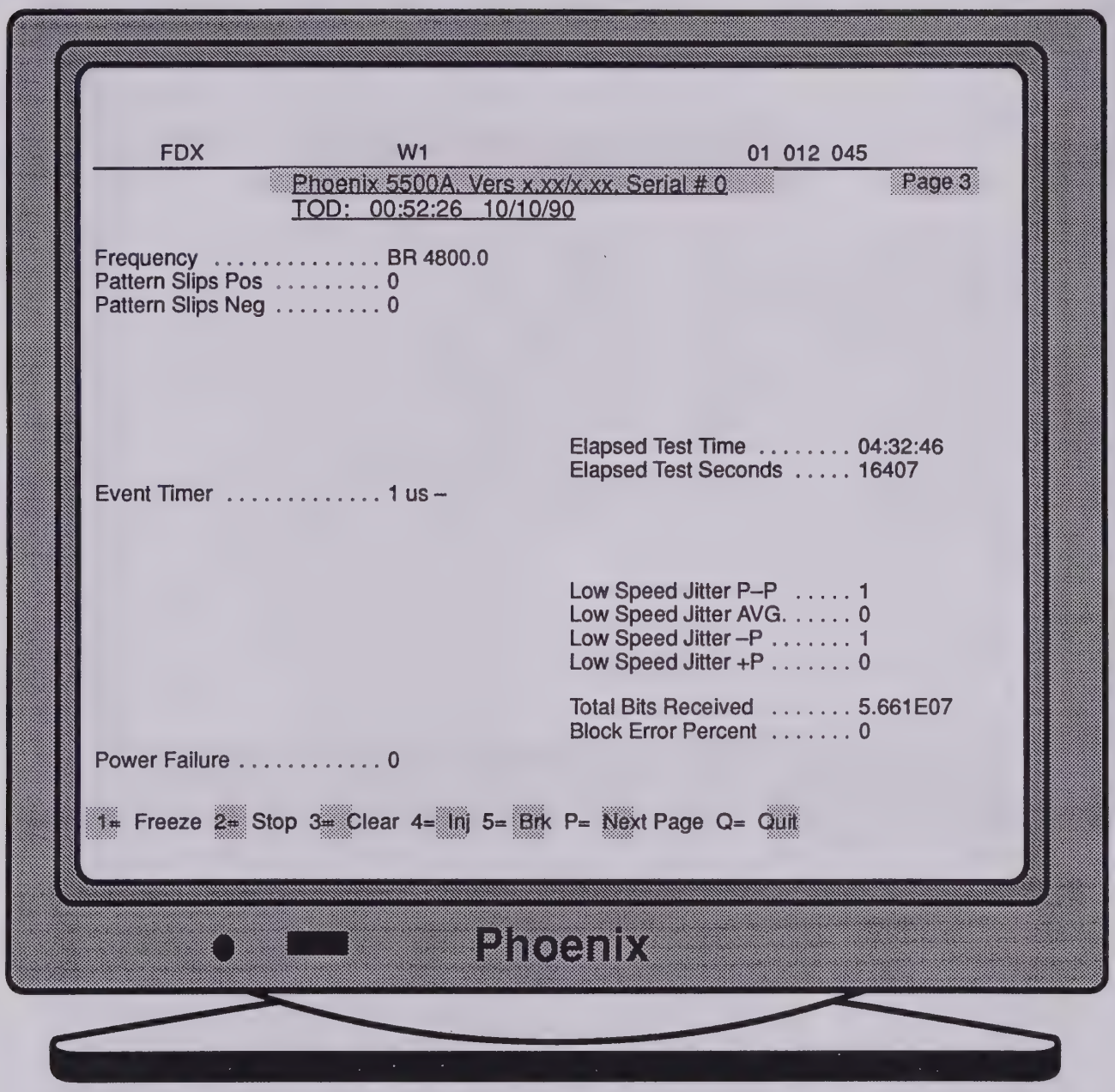
FDX W1 01 012 045
Phoenix 5500A Vers x.xx/x.xx Serial # 0
Page 3
TOD: 00:52:26 10/10/90
Frequency . . . . . BR 4800.0
Pattern Slips Pos 0
Pattern Slips Neg 0
Elapsed Test Time 04:32:46
Elapsed Test Seconds 16407
Event Timer . . . . . 1 us –
Low Speed Jitter P–P 1
Low Speed Jitter AVG. 0
Low Speed Jitter –P 1
Low Speed Jitter +P 0
Total Bits Received 5.661E07
Block Error Percent 0
Power Failure 0
1= Freeze 2= Stop 3= Clear 4= Inj 5= Brk P= Next Page Q= Quit
Phoenix

Figure 5–4. 5500A Remote "Big Screen" Display – Page 3.

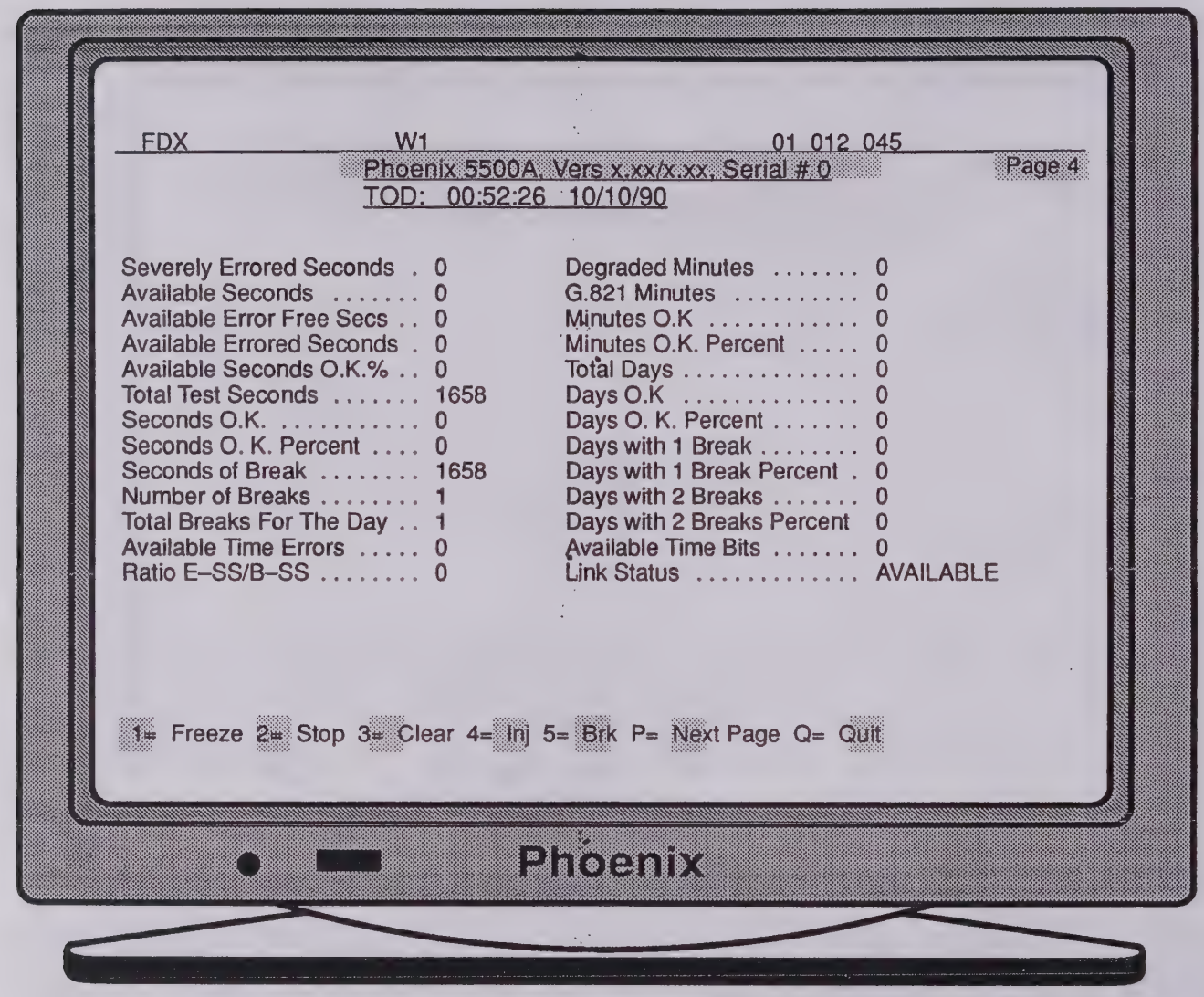
FDX W1 01 012 045
Phoenix 5500A, Vers x.xx/x.xx, Serial # 0
Page 4
TOD: 00:52:26 10/10/90
Severely Errored Seconds . 0
Available Seconds 0
Available Error Free Secs .. 0
Available Errored Seconds . 0
Available Seconds O.K.% .. 0
Total Test Seconds 1658
Seconds O.K. 0
Seconds O. K. Percent 0
Seconds of Break 1658
Number of Breaks 1
Total Breaks For The Day .. 1
Available Time Errors 0
Ratio E–SS/B–SS 0
Degraded Minutes 0
G.821 Minutes 0
Minutes O.K 0
Minutes O.K. Percent 0
Total Days 0
Days O.K 0
Days O. K. Percent 0
Days with 1 Break 0
Days with 1 Break Percent . 0
Days with 2 Breaks 0
Days with 2 Breaks Percent 0
Available Time Bits 0
Link Status ..... AVAILABLE
1= Freeze 2= Stop 3= Clear 4= Inj 5= Brk P= Next Page Q= Quit
Phoenix

Figure 5–4. 5500A Remote "Big Screen" Display – Page 4.

Chapter 6 – Performance Monitoring

6.0 INTRODUCTION

The basic measurement is bit error rate; the number of errors detected during the transmission of a large number of bits in a specially–selected pseudorandom pattern (to permit maximum stressing of all units in the network).

The two drawbacks to error–rate testing are; 1, the time it takes; and 2, the requirement to remove the circuit from use during the testing. Normal spans exhibit error rates in the range of one error in 100,000 bits to one in 10,000,000 bits. It takes a 4800 bps circuit more than three minutes to transmit a million bits of data, and therefore to acquire meaningful measurements, tests must be run for an hour or more. During that hour, specific events, such as a lightning storm near a switching center, can so disrupt normal statistics that test reruns are relatively common requirements.

The G.821 performance evaluation package allows the operator to monitor the performance of the span/equipment being tested in accordance with CCITT Recommendation G.821 without removing the circuit from active use. These measurements are based on time. The total time of the test is divided into increments of time by breaks. A break is defined as a period, measured in seconds, which begins with ten consecutive seconds that are characterized by an error ratio greater than the established threshold (STHR). These errored seconds are referred to as severely errored seconds (SES). A break ends when there have been ten consecutive non–severely errored seconds. This is illustrated in Figure 6–1. The period of time, from the first of the ten severely errored seconds to the first of the ten non–severely errored seconds, is referred to as unavailable time, or a break (the circuit is also considered non–available at that time.)

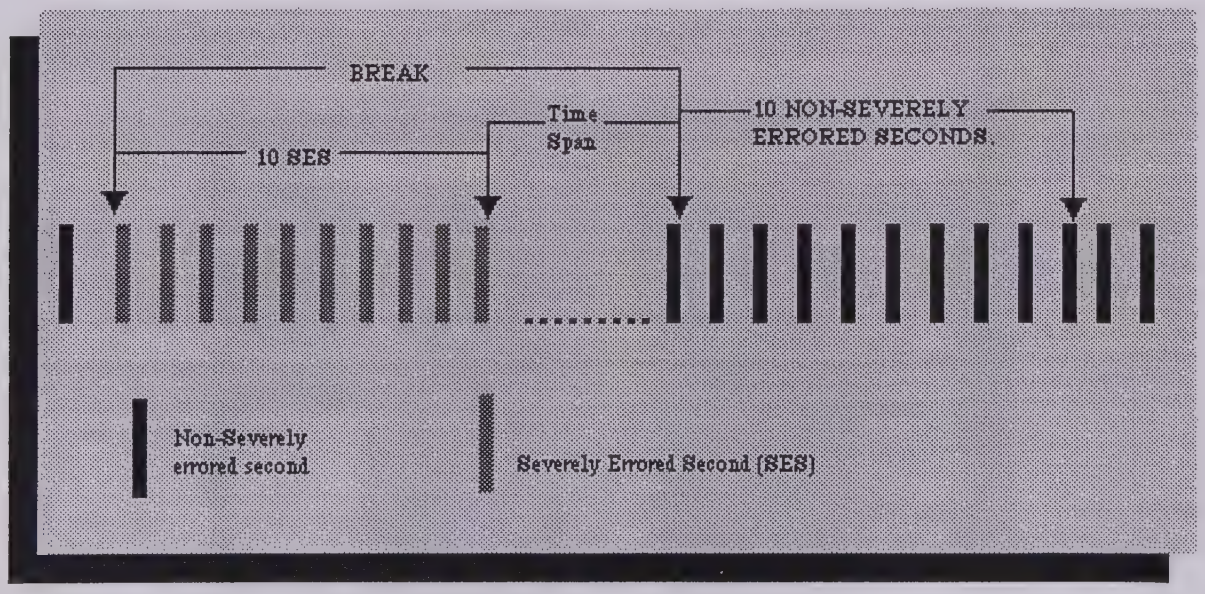

Figure 6–1. Timing Relationships in G.821 Performance Monitoring.

Subtracting non–available time from total test time results in available time. Thus the G.821 testing period is divided into available and non–available time. The 5500A has been designed to operate on the basis of the available and non–available time to provide the operator with all of the significant G.821 parameters.

6.1 OPERATION

It is recommended that sections 2, 3, and 4 of this manual be read prior to G.821 testing.

Measurement of the G.821 parameters is accomplished by selecting the G.821 display, shown in Figure 6–2. The G.821 display is located under the BIG BERT display in the menu matrix. The top line of the display is used to indicate the name of the menu (G821), if the 5500A is in the RUN mode, and the word **BREAK** appears during break periods (nothing is displayed during available time). To bring the G.821 display to the screen, proceed as follows:

1. Turn on the 5500A.
2. Press the **RECALL** key on the front panel of the 5500A one time to bring the HELP menu to the display.
3. Press the **E** key on the front panel HEX keypad.
4. Press the **GO TO** softkey on the front panel of the 5500A.
5. The G.821 display, as shown in Figure 6–9, should now be on the display.

6.2 PARAMETER DEFINITIONS

The G.821 parameters and their definitions follow. Any of the listed parameters may be selected to be displayed on the G.821 display by moving the cursor over the desired location and toggling the SELECT keys until the desired parameter appears (in Figure 6–2 the cursor is shown on the location where DAYS has been chosen). The EBPS (explicit bits per second) is set by the 5500A. The STHR and MTHR parameters are permanently displayed to permit the operator to select their values by placing the cursor over the desired field. The STHR and MTHR values are entered by using the HEX keypad on the front panel, while the EBPS value is entered by scrolling to the desired value using the SELECT keys.

TS Total seconds of test. The accumulation begins when the tester achieves the first synchronization. Subsequent losses/gains of synchronization will not affect the measurement. A test cannot be started on an unavailable circuit.

SES Severely errored seconds. Seconds that are characterized by a high error ratio (STHR). The value specified in the G.821 definition is .001 (1 bit error in every 1000 bits), but due to the fact that customers need to be able to set this threshold (STHR) to a lower value, the 5500A allows the operator to specify the number of errors (STHR) that determines a SES.

STHR Severely errored second threshold. This is the minimum number of errors that determine a

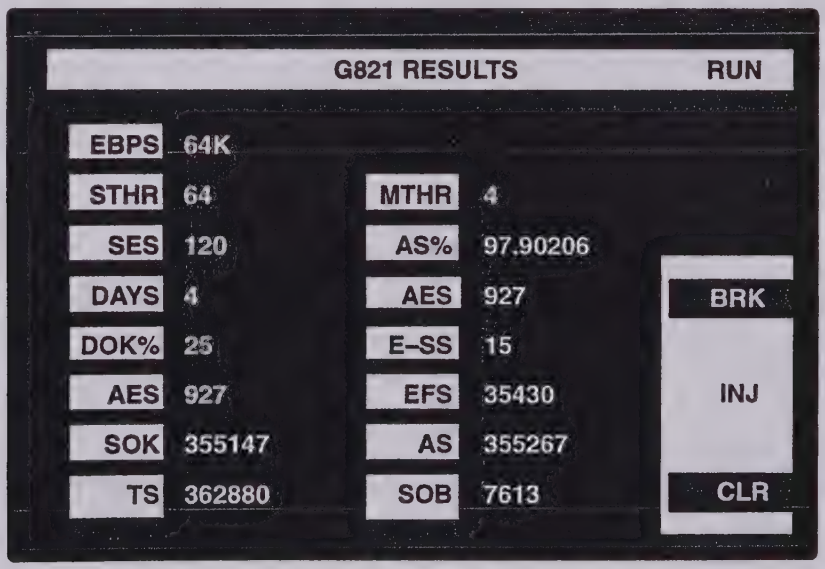

Figure 6–2. G.821 Menu.

SES. Operator entered from front panel or from the remote port.

SOB Unavailable seconds (or seconds of break). The sum of every period of unavailable time experienced by the circuit. (Unavailable time is defined in paragraph 6.0.)

MIN Number of available time minutes. Available time minutes are total minutes less degraded minutes (DM).

DM Degraded minutes. Available time is divided into packets of sixty seconds, or one minute. The sum of the errors, relative to 60 seconds, is computed and used to characterize the minute. The minute is considered degraded if its total error sum is greater than the threshold (MTHR) that is also programmable by the operator. (G.821 defines the error ratio threshold as 10–6 which would be 4 at a 64K EBPS).

AS Available seconds. The sum of every period of available time.

AES Available errored seconds. The number of seconds, in available time, that are errored.

In addition to the above CCITT parameters, the following parameters are also evaluated and available for display. This particular set of parameters was selected primarily for testing procedures at British Telecom.

Contact Phoenix Microsystems Customer Service if your needs are not met by these parameters.

EFS Available error free seconds. The number of seconds, in available time, that are error free.

$$EFS = AS - AES$$

EFS% Percent of EFS. The percentage of available error free seconds in relation to the total number of available seconds.

$$EFS\% = \frac{EFS}{AS} * 100$$

SOK Seconds, in available time, characterized by a number of errors less than the selected value of STHR. (G821 spec error ratio as 10–3 which is STHR of 64 with EBPS of 64K)

SOK% Percent of SOK. The percentage of SOK in relation to the total number of available seconds.

$$SOK\% = \frac{SOK}{AS} * 100$$

MOK Minutes, in available time, characterized by a number of errors less than the selected value of MTHR. (G.821 spec error ratio at 10–6 which is MTHR of 4 with EBPS of 64K)

MOK% % of MOK. The percentage of MOK in relation to the total number of minutes.

$$MOK\% = \frac{MOK}{MIN} * 100$$

AS% Percent of AS. The percentage of available time in relation to the total test time.

$$AS\% = \frac{AS}{TS} * 100$$

E–SS Total number of errors counted during available time, excluding severely errored seconds.

B–SS Total number of bits received in available time, excluding severely errored seconds.

R–SS (E–SS)/(B–SS). The error ratio relative to available time, excluding severely errored seconds.

NOB Number of breaks. This counter is incremented any time a new period of unavailable time is detected.

TBFD Total number of breaks for the day. This counter is reset daily. It is incremented each time a new period of unavailability (break) is detected unless the break crosses the day boundary. In that case, the following rules apply (refer to Figure 6–3).

1. A break is always counted for one of the days.

2. If the break lasts for 10 or more seconds in both days, then it is counted in both days.

DAYS Total number of days of the test.

DOK Number of break free days. A day of test in which no break has been experienced.

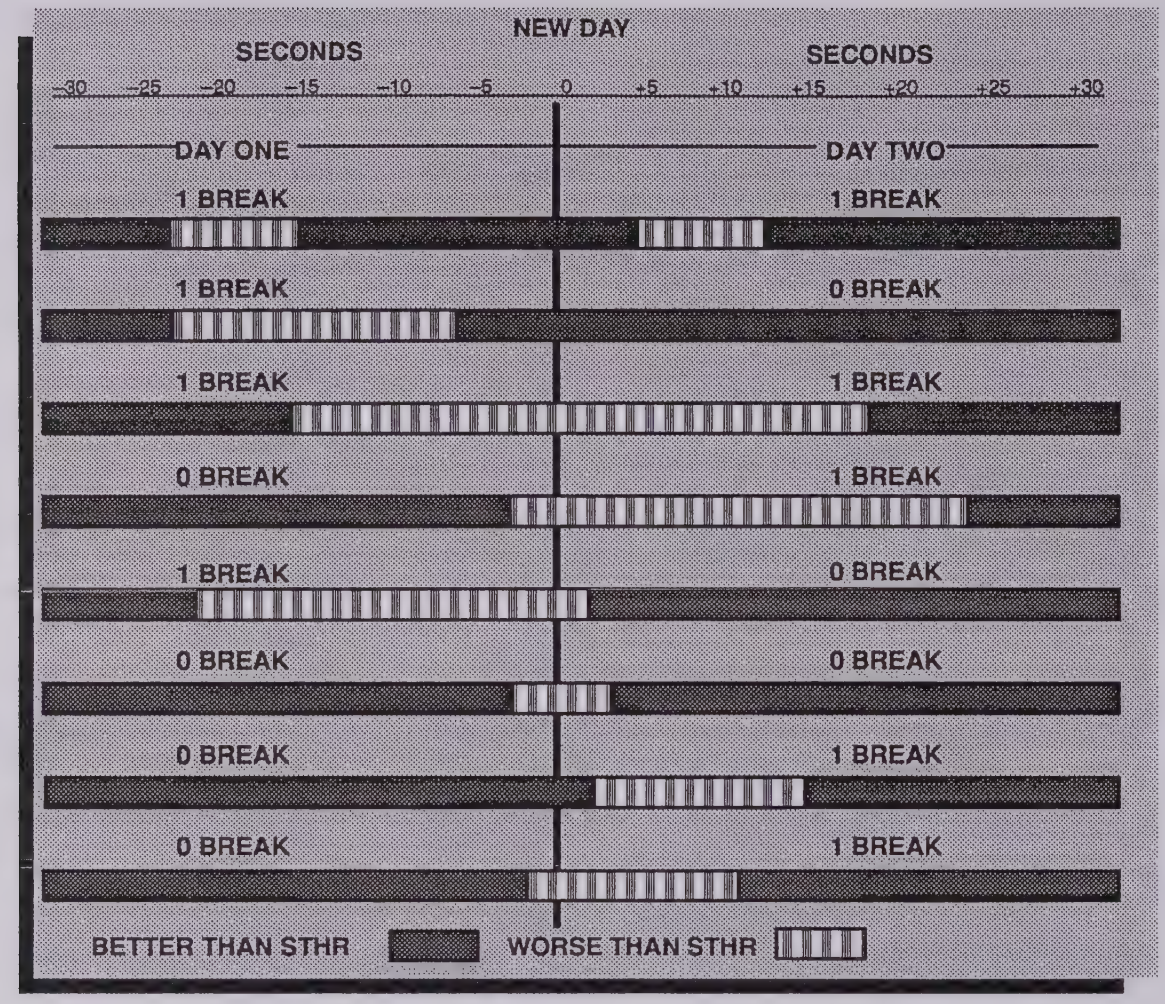

Figure 6–3. Breaks Crossing Day Boundary.

DOK% Percent of DOK. The percentage of break free days in relation to the total number of days of test.

$$DOK\% = \frac{DOK}{DAYS} * 100$$

DB1 The number of days with one break. A day of test in which only one break has been experienced.

DB1% Percent of DB1. The percentage of days with one break in relation to the total number of days of test.

$$DB1\% = \frac{DB1}{DAYS} * 100$$

DB2 The number of days with two or more breaks. A day of test in which two or more breaks occur.

DB2% Percent of DB2. The percentage of days with two or more breaks in relation to the total number of days of test.

$$DB2\% = \frac{DB2}{DAYS} * 100$$

EBPS Explicit bits per second. This parameter is used to calculate E–SS, B–SS, and R–SS. It is automatically set to the bit rate displayed in the format menu.

MTHR Degraded minute threshold. This is the minimum number of errors that determine a DM. Operator entered from front panel or from the remote port.

6.3 REMOTE OPERATION

All of the operating functions of the 5500A G.821 menu may be addressed via the remote ports. (see chapters 2 and 5 of this manual) Specifically, the list of G.821 parameters and commands can be read over the remote port by invoking the "?" command. The last page of the Help Menu (which appears after entering the "?") lists the G.821 parameters as shown in Figure 6–4. The test results can be viewed on the remote UPDATE screen which displays all the test parameters in real time. The G.821 parameters appear on page three of this display as shown in Figure 6–5. The displayed fields on the G821 display screen can be modified by means of the GF1 thru GF12 commands (these relate to the position on the 5500A CRT screen as shown in Figure 6–6. **ALL** of the G.821 parameters printed when the G.821 field on the Print Menu (Figure 6–7) is selected.

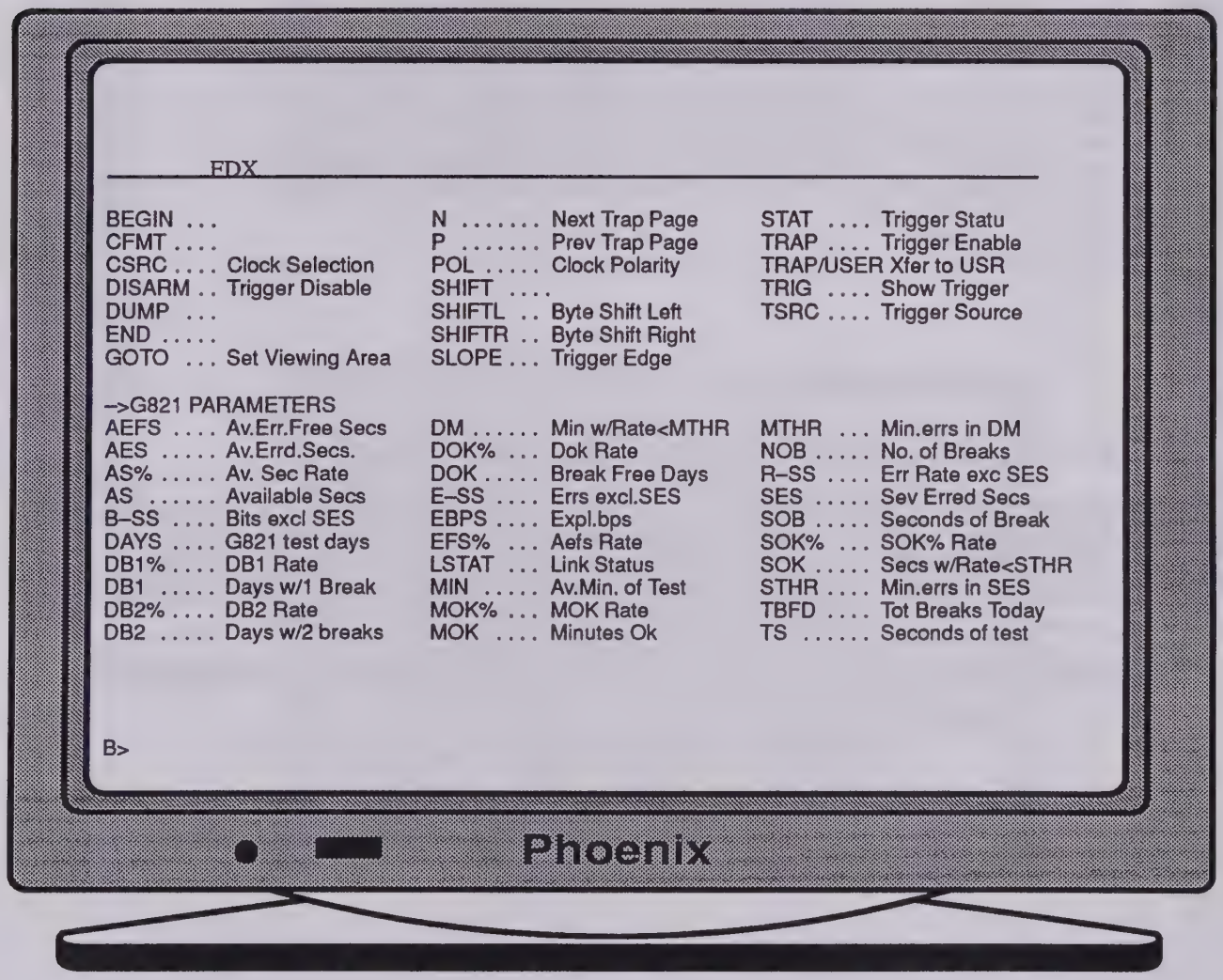
FDX
BEGIN ...
CFMT ....
CSRC .... Clock Selection
DISARM .. Trigger Disable
DUMP ...
END .....
GOTO ... Set Viewing Area
N ..... Next Trap Page
P ..... Prev Trap Page
POL ..... Clock Polarity
SHIFT ....
SHIFTL .. Byte Shift Left
SHIFTR .. Byte Shift Right
SLOPE ... Trigger Edge
STAT .... Trigger Statu
TRAP .... Trigger Enable
TRAP/USER Xfer to USR
TRIG .... Show Trigger
TSRC .... Trigger Source
->G821 PARAMETERS
AEFS .... Av.Err.Free Secs
AES ..... Av.Errd.Secs.
AS% ..... Av. Sec Rate
AS ..... Available Secs
B–SS .... Bits excl SES
DAYS .... G821 test days
DB1% .... DB1 Rate
DB1 ..... Days w/1 Break
DB2% .... DB2 Rate
DB2 ..... Days w/2 breaks
DM ..... Min w/Rate<MTHR
DOK% ... Dok Rate
DOK ..... Break Free Days
E–SS .... Errs excl.SES
EBPS .... Expl.bps
EFS% ... Aefs Rate
LSTAT ... Link Status
MIN ..... Av.Min. of Test
MOK% ... MOK Rate
MOK .... Minutes Ok
MTHR ... Min.errs in DM
NOB ..... No. of Breaks
R–SS .... Err Rate exc SES
SES ..... Sev Erred Secs
SOB ..... Seconds of Break
SOK% ... SOK% Rate
SOK ..... Secs w/Rate<STHR
STHR .... Min.errs in SES
TBFD .... Tot Breaks Today
TS ..... Seconds of test
B>
Phoenix

Figure 6–4. G.821 Parameters as Listed on Remote Help Menu.

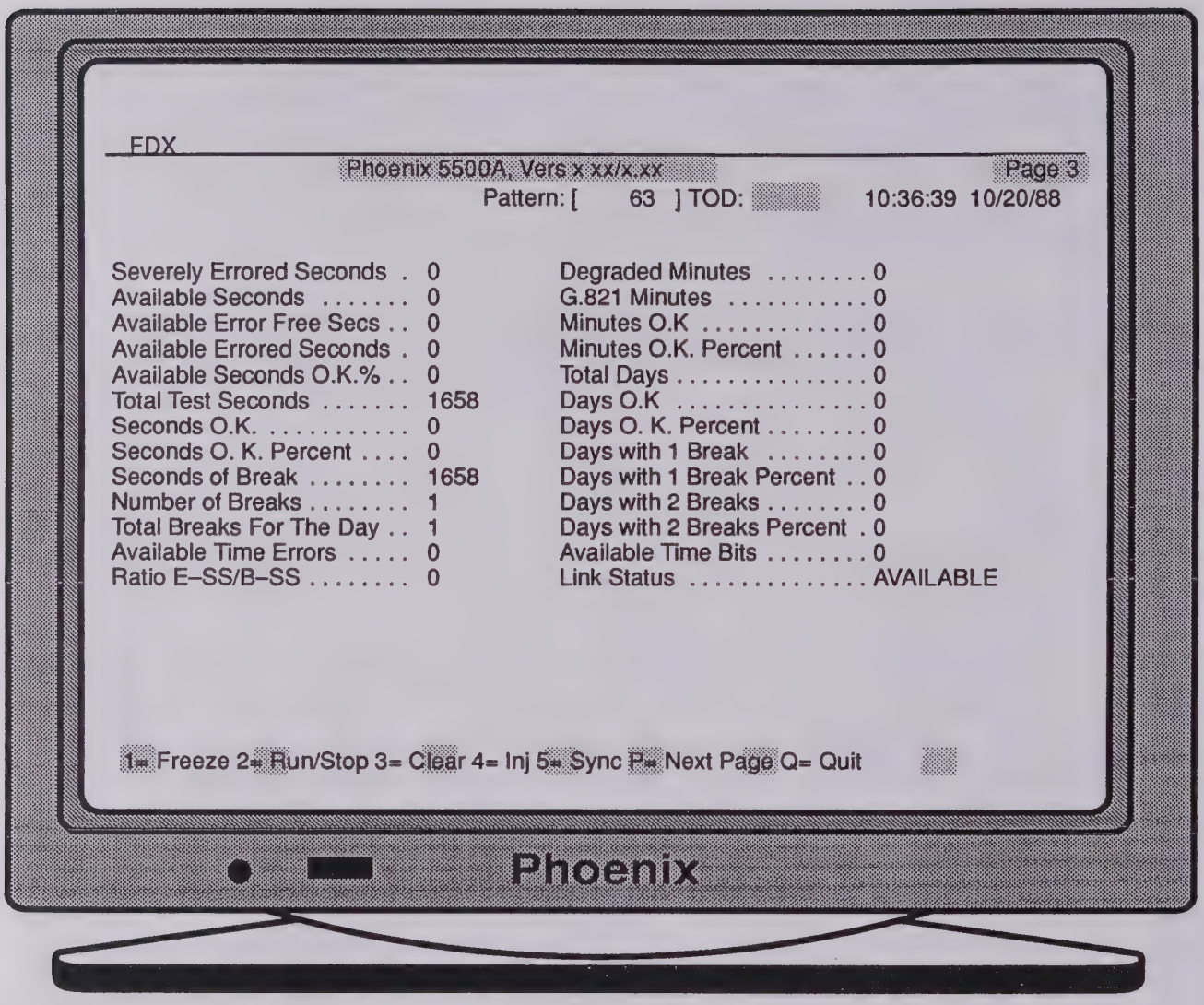
EDX
Phoenix 5500A, Vers x xx/x.xx
Page 3
Pattern: [63] TOD:
10:36:39 10/20/88
Severely Errored Seconds . 0
Available Seconds 0
Available Error Free Secs .. 0
Available Errored Seconds . 0
Available Seconds O.K.% .. 0
Total Test Seconds 1658
Seconds O.K. 0
Seconds O. K. Percent 0
Seconds of Break 1658
Number of Breaks 1
Total Breaks For The Day .. 1
Available Time Errors 0
Ratio E–SS/B–SS 0
Degraded Minutes 0
G.821 Minutes 0
Minutes O.K 0
Minutes O.K. Percent 0
Total Days 0
Days O.K 0
Days O. K. Percent 0
Days with 1 Break 0
Days with 1 Break Percent .. 0
Days with 2 Breaks 0
Days with 2 Breaks Percent . 0
Available Time Bits 0
Link Status ..... AVAILABLE
1= Freeze 2= Run/Stop 3= Clear 4= Inj 5= Sync P= Next Page Q= Quit
Phoenix

Figure 6–5. Real Time Remote Screen, Page 3.

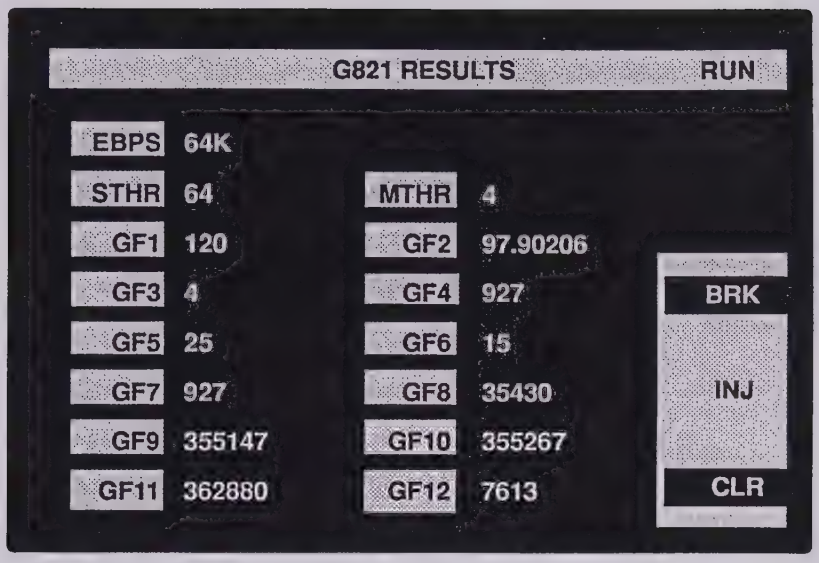

Figure 6–6. G.821 Menu.

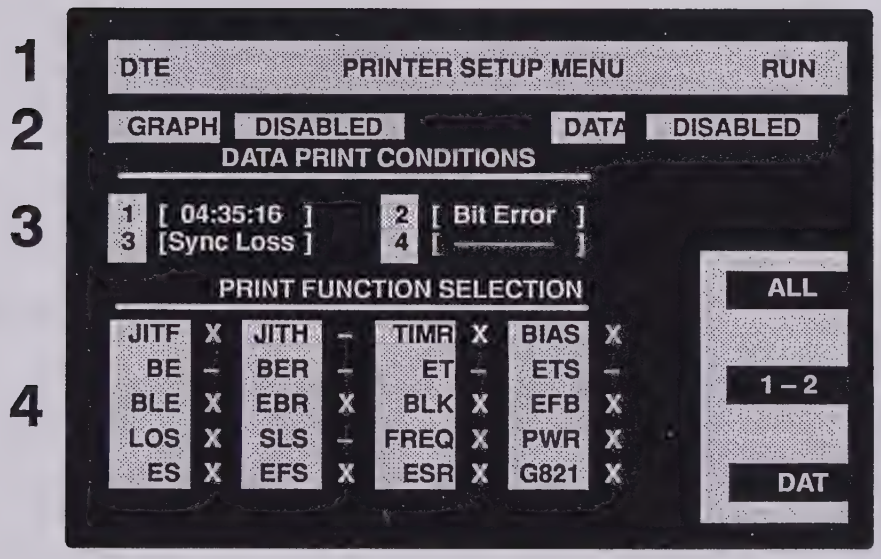

Figure 6–7. 5500A Printer Setup Menu.

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Chapter 7 – Maintenance

7.0 INTRODUCTION

This section of the manual provides all the necessary instructions for a well trained technician to perform maintenance and test procedures for the Model 5500A test set. Product specifications are provided in Appendix A.

Recommended calibration frequency for the 5500A test set is 1 year.

7.1 MODEL 5500A MAINTENANCE

The 5500A is comprised of a chassis, power supply, and four printed circuit boards. The four PC boards are the 5500A control board, video control board, front panel display/keypad board, and an interface board. The interface board may be one of several plug–in modules, allowing the 5500A to operate in a variety of configurations.

Each 5500A is supplied with a 3.6V Ni–Cad battery and necessary control logic to back up the read/write memory during power down.

7.1.1 PROM Replacement

When upgrading your 5500A software, it will be necessary to remove and replace the PROM chips in your unit with PROMs which contain the new software. The 5500A currently uses six PROMs (U1, U2, U3, U4, U8, and U9 on the PROM board and PROM U1 on the video board), although provisions are made on the PROM board (7–5500A–413–2) for 10 PROMs. The PROM board (Figure 7–1) is located on the top of the main control board and is designed for easy removal of PROMs. PROM locations are illustrated in Figure 7–2 and Figure 7–3.

To maintain your warranty, return the removed PROMs in the container that held the new PROMs, along with the 5500A serial number, to the following address.

Customer Service Manager
PROM CR
Phoenix Microsystems, Inc.
991 Discovery Drive
Huntsville, AL 35806

7.1.2 Ni–cad Battery Replacement

The PMB series rechargeable memory back–up batteries provide from five to seven years of operation of a constant trickle charge. Phoenix recommends changing the Ni–cad batteries every three years.

NOTE All preprogrammed settings will be lost when Ni–cad batteries are replaced. Be prepared to reinstall programmed settings after battery replacement.

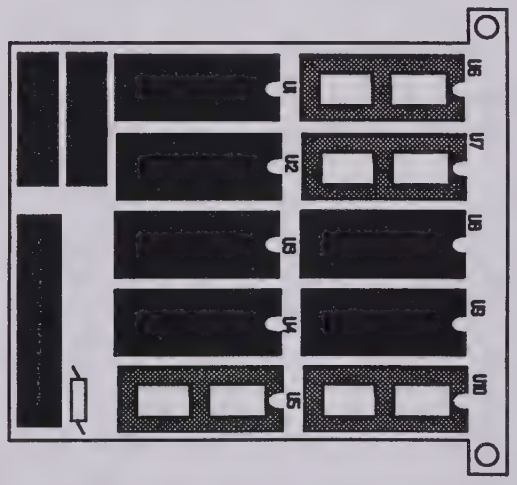


Figure 7–1. Model 5500A PROM Card.

The following equipment is required for Ni–cad battery replacement.

(1) Phillips head screwdriver

(1) Soldering iron

(1) Desoldering tool or wik wire

(2) Batteries, 3.6 volt Ni–cad (Phoenix part number 10–00003, PMB 3.6B)

To replace the Ni–cad batteries (Figure 7–3), proceed as follows.

1. Remove chassis form main housing.
2. Remove six screws and all connectors attached to the control board.
3. Remove four screws and all connectors attached to the video board.
4. Locate and replace the 3.6 Ni–cad battery on each board.
5. Reassemble the test set.

7.1.3 Video Board Calibration

The following equipment is required to calibrate the video board.

(1) Frequency counter or oscilloscope

(1) Small flat head screwdriver or trimmer adjustment tool

To calibrate the video board, proceed as follows.

1. Monitor either U18–1 or R9–1 with the oscilloscope or counter.
2. Adjust the time of day clock at C29 for 64 Hz, ±5%.

7.1.4 Power Supply Calibration

No adjustments are required for the power supply. Voltages may be verified using a digital multimeter.

To verify voltages, proceed as follows:

1. Locate the J8 connector on the control board of the 5500A.
2. Place the black lead (ground) of the digital multimeter to J8 pin 6, 7, 8, or 9.
3. Place the red lead (positive) to the following pins and verify voltages.

J8 pin 1	–5 volts	±3%
J8 pin 2	–5 volts	±3%
J8 pin 3	+5.1 volts	±2%
J8 pin 10	+12 volts	±3%
J8 pin 11	–12 volts	±3%
J8 pin 12	–30 volts	±3%

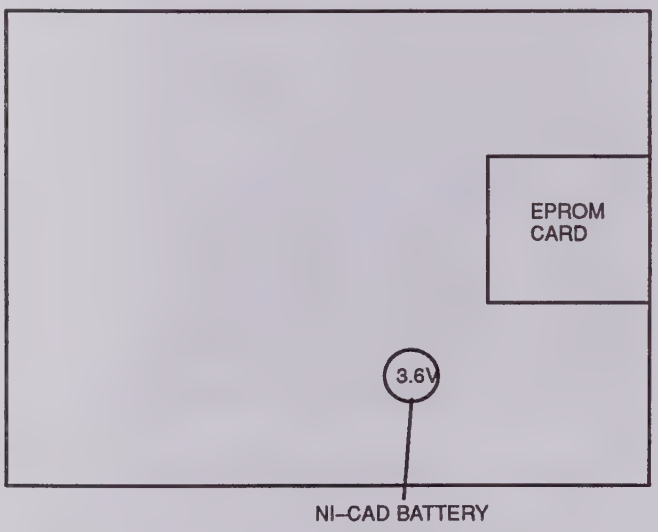


Figure 7–2. PROM Card and Battery Location on the Control Board 5500–393–1.

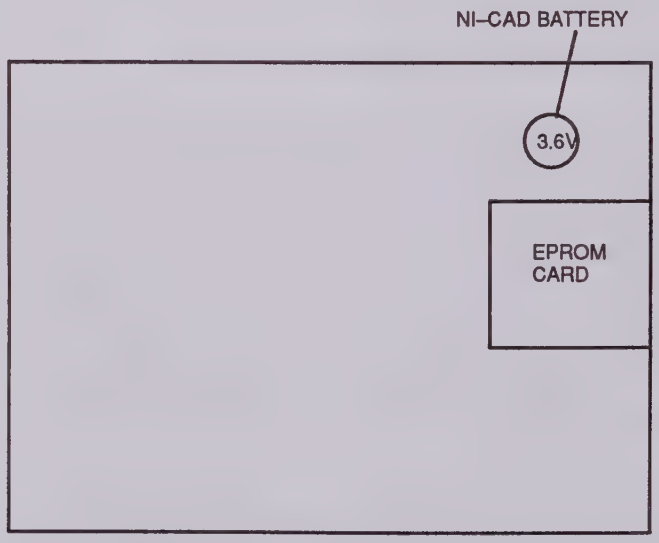


Figure 7–3. EPROM Card and Battery Location on the Video Board 5500N–023–1.

7.1.5 Control Board

The following equipment is required to calibrate the 5500A–393–1 control board.

(1) Precision Frequency Counter

(1) 100 MHz Oscilloscope

(1) Tuning Tool

(1) Phillips Head Screwdriver

1. Remove chassis from main housing.
2. Insert RS–449 Interface Module and allow the 5500A to warm up for one hour prior to start of calibration.
3. Connect the frequency counter to U66, pin 13 (Figure 7–4).

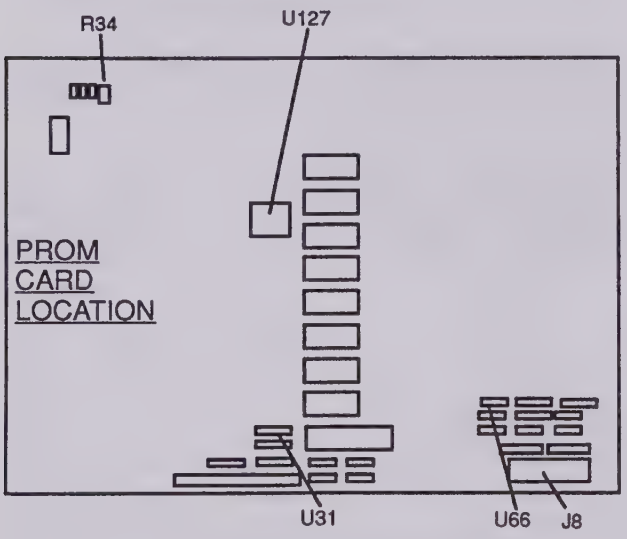
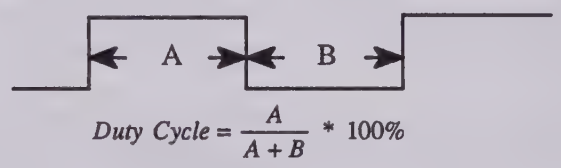


Figure 7–4. 5500A–393–1 Control Board.

4. Verify the reading on the frequency counter is 16,000,000 Hz ±5 Hz. If reading is within tolerance, proceed to step 5.
5. Locate U127. Using tuning tool, adjust tuning screw until the frequency counter reading is 16,000,000 ± 5 Hz.
6. Set the frequency on the BERT Format menu to 13 MHz.
7. Connect the oscilloscope to U31, pin 3. The signal on the oscilloscope should have a 50% duty cycle as shown below.



$$Duty\ Cycle = \frac{A}{A+B} * 100\%$$

If the signal duty cycle is not 50%, adjust R34 until a 50% duty cycle is obtained.

8. Remove the frequency counter and oscilloscope connections from the control board. Reassemble the test set.
9. If any problems were encountered while performing this procedure, contact Phoenix Customer Service at 1–800 866–8480, Ext. 255.

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Chapter 8 – Options

8.0 INTRODUCTION

The section of the manual contains brief descriptions of the options available for use with the Model 5500A test set. A separate manual is provided with each option. Table 8–1 lists the options and the applicable manual part number.

8.1 INTERFACE MODULES

The logic required to operate in the Sync and Async modes is contained within the 5500A. To match the 5500A TTL logic to the various standards used throughout the world, various I/O (input/output) modules are available for the 5500A. These modules are designed to slide into the I/O slot in the rear panel of the 5500A; no other connections or modifications are required. The 5500A displays the proper menus for the installed module. The following paragraphs provide a brief description of each of the modules currently available. For additional information contact your Phoenix Representative or Phoenix Customer Service at 1–800–866–8480, Ext 255.

Table 8–1. Model 5500A Options/Manual Part Numbers.

OPTION	PART NUMBER	MANUAL
RS–232 I/O	F–5500–200—11	34–00037
V.35 I/O	F–5500–300—11	34–00038
RS–499/MIL STD 188 I/O	F–5500–450—11	34–00039
TTL I/O	F–5500–500—11	34–00040
EIA 530	F–5500–530A–1	34–00141
DDS I/O (with secondary channel)	F–5500–538B—11	34–00176
DS0/DS0A I/O	F–5500–539A—11	34–00042
DS0/DS0A I/O (with secondary channel)	F–5500–539B—11	34–00175
I/O Control for MSU	F–5500–555—11	34–00043
T1–C Unframed I/O	F–5500–600A–11	34–00044
Bi–Phase I/O	F–5500–605A–11	34–00045
Fractional T1 I/O	F–5500–636A–110	34–00092
T2 Unframed I/O	F–5500–700A–11	34–00048
CCITT G.703 (8.448) I/O	F–5500–805A–11	34–00051
CCITT G.703 (64 Kbps) I/O	F–5500–810A–11	34–00049
CCITT 64Kbps x N I/O (with drop and insert)	F–5500–836B–110	34–00159
Jitter Measurement at T1 – JO2 Jitter Option	F–5500–636A–111	34–00054
Jitter Measurement at 2.048 – JO2 Jitter Option	F–5500–836A–111	34–00055

8.1.1 RS–232 (5500–200)

The 5500–200 RS–232 I/O module performs the electrical and mechanical interface between EIA RS–232 standard signals and the 5500A.

The module has two 25–pin subminiature 'D' type connectors; normally male for DCE and female for DTE. DCE/DTE emulation is electronically switchable from the 5500A front panel or via command from a remote terminal over either remote control port.

8.1.2 V.35 (5500–300)

The 5500–200 V.35 I/O module performs the electrical and mechanical interface between CCITT V.35 recommended standard signals and the 5500A.

The module has two V.35 connectors; male for DCE and female for DTE. DCE/DTE emulation is electronically switchable from the 5500A front panel or via command from a remote terminal over either remote control port.

8.1.3 RS–449 (5500–450)

The 5500–450 RS–449 MIL–188–114 module is designed to provide the balanced (RS–422) and unbalanced (RS–423) electrical interfaces of RS–449 and MIL–188–114. The electrical interface parameters of MIL–STD–188–114 are equivalent to RS–449 parameters with the exception of the balanced generator offset voltage which is restricted to a value of ±0.4 volts maximum for MIL–STD–188–114 (RS–449 permits ±3.0 volts maximum). The 5500–450 module balanced generators are balanced to ground with an offset voltage of less than ±0.4 volts. Therefore, this module is completely compatible with both MIL–STD–188–114 and RS–449.

8.1.4 TTL (5500–500)

The 5500–500 TTL module has the same physical connectors and pin assignments as the 5500–200 RS–232 I/O module; however, the logic is inverted on all data, clock, and control lines (relative to standard EIA RS–232 logic convention).

8.1.5 (5500–530A)

The 530/531 Universal module is designed to permit the 5500A to be configured to test both DCE and DTE devices. The logic required to operate in SYNC and ASYNC mode is located within the 5500A itself. The interface module performs the mechanical and electrical interfacing of the EIA RS–232C/D, EIA 530 balanced and unbalanced, V.11, V.10, EIA 422, EIA 423, and MIL–STD–188/114 balanced and unbalanced standard signals to the TTL level signals used within the 5500A.

8.1.6 DDS Interface Module (5500–538B)

The 5500–538B DDS module tests digital data systems (DDS) at the DS–CS level (Customer Service rate) and any non–DDS circuits which use DSU/CSUs as short haul modems. This module supports service rates of 2.4, 4.8, 9.6, 19.2, and 56 kbps, secondary channel capability, 64 kbps clear channel capability (56 kbps secondary channel service only), BERT through DTE interface or DDS interface, asynchronous and synchronous modes for non–secondary channel service (DDS and DTE interface), and synchronous primary channel and secondary channel (full secondary channel bandwidth is tested, N=3) testing for secondary channel service (DDS interface only). The 5500–538B is equipped with an extended range receiver (–45 dB @ 56 kbps, –40 dB @ subrates) and has internal, user, and recovered clock modes.

Additional features and the operation of the 5500–538B module are provided in Phoenix manual 34–00176.

8.1.7 DS0/DS0A (5500–539A)

The 5500–539A module allows the 5500A to test digital data systems (DDS) at the DS0 level (64 kbps). This module may be used for loopback or straightaway testing at data rates of 2.4, 4.8, 9.6, or 56 kbps. A 64 kbps data rate is provided for straightaway or manual loopback testing of the full 64 kbps (clear channel testing). The module transmits and receives DS0A formatted signals and may be configured for bipolar, logic near, or logic far signals.

8.1.8 DS0/DS0A/DS0B Interface Module (5500–539B)

The 5500–539B DS0 module tests digital data systems (DDS) at the DS0 level (64 kbps). This module is designed for installation and maintenance testing of the DDS at the DS0/DS0A/DS0B level in the Central Office environment and may be used for loopback or straightaway testing at data rates of 2.4, 4.8, 9.6, 19.2, 28.8, 38.4, 48, or 56 kbps. A 64 kbps data rate is also provided for straightaway or manual loopback testing of the full 64 kbps (clear channel testing). The 5500–539B is designed to support DDS tests described per TA–TSY–000055, April 1987. Secondary channel capability, secondary channel BERT patterns, and

simultaneous primary and secondary channel BERT are also included.

Additional features and the operation of the 5500–539B module are provided in Phoenix manual 34–00175.

8.1.9 MSU Control Module (5500–555)

When used with the 5500–MSU (Module Switching Unit), the MSU Control Module provides the capability to select up to 16 interface modules for use with the 5500A. The system is modular and may be expanded to switch from as few as two modules up to the maximum of 16 modules via the 5500–MSU that switches up to 4 modules each.

8.1.10 DS–1/DS–1C (5500–600)

The 5500–600 module enables the 5500A to test T–carrier systems operating at 1.544 Mbps (DS–1) and 3.152 Mbps (DS–1C) rates in accordance with applicable Bell System and U. S. Telephone Association specifications for signals present at the DSX–1 and DSX–1C cross–connect points. The module functions with signals at normal transmit and receive levels as well as with monitor level signals at the DSX points.

8.1.11 Bi–phase (5500–605)

The 5500A–605 module allows the 5500A to test Bi–phase, modulated, digital interfaces. This module may be used for stand alone testing of customer equipment in a terminating mode or for monitoring of bi–phase modulated digital lines on a non–interfering high impedance, bridged mode.

8.1.12 DS1 (T1) (5500–636)

The 5500–636 module enables the 5500A to test all types of T1 carrier equipment with D4, ESF (Extended Super Frame), or SLC®96 framing as well as unframed T1 equipment. The 5500–636 also permits the user to select the individual DS0 channel(s) desired for testing. The line format is selectable for either AMI or B8ZS. The module includes a high performance ALBO/Clock Recovery circuit with wide dynamic range (+6 dBdsx to –27 dBdsx) and exceptional jitter tolerance (>10 UI peak–to–peak @ 600 Hz, QRSS pattern). The receiver may be operated in a bridge, monitor, or terminate mode.

8.1.13 T2 (5500–700)

The 5500–700 module enables the 5500A to test T–carrier systems operating at 6.312 Mbps rates (T2). The module provides two output levels to simulate the 6.312 Mbps signals found at both the terminal equipment and at the DSX–2 cross connect, as well as providing the capability to monitor the signal levels originating at both locations. The module operates with the T2 serial, bipolar (return–to–zero) pulses that utilize the Bipolar with 6 Zero Substitution (B6ZS) line code. In addition, the 5500–700 may be configured to provide AMI line code via switch selection on the module.

The 5500–700 enables the 5500A to generate and receive T2 serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consists of Western Electric Company type 310 compatible jacks for transmit and receive.

8.1.14 G.703 8448 kbps (5500–805)

The 5500–805 module enables the 5500A to test data communication systems operating at G.703 8448 kbps rates in accordance with the CCITT G.703 Recommendation. The module provides the capability to transmit and receive data at the 8448 kbps rate, in either HDB3 or AMI line code formats, utilizing bipolar transmission.

The mechanical interface between the module and the system under test consists of; BNC type connectors for transmit and receive data, each with a separate grounding lug that permits the user to terminate the coaxial shield if desired; and a 15–pin subminiature D–type connector for transmit and receive data (used by some modem manufacturers) whose pins are in parallel with the transmit and receive BNC connectors.

8.1.15 G.703 64 kbps (5500–810)

The 5500–810 module enables the 5500A to test data communication systems operating at G.703 64 kbps rates in accordance with the CCITT G.703 Recommendation. The module provides the capability to transmit and receive data and clock signals in any of the three modes of operation specified in CCITT Recommendation G.703; codirectional interface mode, centralized clock interface mode, and both the line side and service side of the codirectional interface mode. In addition, the 5500–810 module permits the 5500A to provide octet timing, injection, and detection of bipolar violations, clock error detection, codirectional code violation detection, byte synchronous user pattern transmission, high impedance monitoring of live traffic in the receive direction, low level and high level transmission, and internal loopback.

The mechanical interface between the module and the system under test consists of four type 310 compatible jacks for transmit and receive data and clock. A 25–pin D–type connector is wired in parallel with the type 310 jacks.

8.1.16 G.703 2.048 Mbps (5500–836B)

The 5500–836B module enables the 5500A to test framed or unframed N x 56/64 Kbps G.703/G.704 transmission facilities. The line format is selectable for either AMI or HDB3. The module includes a high performance ALBO/Clock Recovery circuit with wide dynamic range and exceptional jitter tolerance. The receiver may be operated in the BRIDGE, MONITOR, or TERMINATE modes.

The 5500–836B features extensive test capabilities for monitoring and troubleshooting "live traffic" circuits. Seven different frame modes are supported: (1) CRC4/PCS0 = Cyclic Redundancy Checksum at 4 bits per word/ Per Channel Signaling Phase 0, (2) CRC4/CCS = Cyclic Redundancy Checksum at 4 bits per word/ Common Channel Signaling, (3) CCS = Common Channel Signaling, (4) PCS0 = Per Channel Signaling Phase 0, (5) PCS1 = Per Channel Signaling Phase 1, (6) IRSM = International Remote Switching Module, and (7) DISABLE. In PCS0 and CRC4/PCS0 the transmitter will align the TS16 Multiframe Alignment Signal (MAS) word with the TS0 Frame Alignment Signal (FAS) word. In the PCS1 mode, the transmitter aligns the MAS word with the TS0 "Not" word. In the CRC4 framing modes, the CRC4 bits and CRC4 framing bits are transmitted over the International bit positions. In DISABLE mode, the data is not frame aligned.

The 5500–836B facilitates special Drop/Insert mode testing which places the 5500–836B in series with a G.703 circuit to insert a test pattern in any channel(s), BERT test or trap any channel(s) (before insertion), and inject bit errors (data or framing) in live traffic.

In addition, the 5500–836B is used for "live traffic" diagnostic testing using the Loop Timed/Not Loop Timed indication, Jitter Measurement with spectral analysis, Alarm status indication, and ISRM data link access. "LOOP TIMED"/"NOT LOOP TIMED" indication is based upon the absence or presence of phase slips between the measured TX reference clock and the measured RX clock (threshold is ± 40UI). The status of BLUE ALARMS, REMOTE ALARMS, Low Level Carrier, and FRAME ALARMS is provided with automatic time stamped printouts of alarm events. Also, when using the 5500A, ISRM data link access (bit 4 of FAS "NOT" word, TS0) is available for either monitoring or sending data link messages with a Phoenix Model 1500 Analyzer/Data Trap, or similar device.

With the addition of the 5500–JO5 high speed jitter option, the 5500–836B module will permit the 5500A to perform high speed jitter analysis with pre–selected data patterns and inject or remove high speed jitter from live traffic.

8.2 JITTER OPTIONS

8.2.1 High Speed T1 (5500A–JO2)

The 5500–JO2 option is a factory installed option which provides the 5500A with jitter measurement and jitter injection capability at the T1 1.544 Mbps rate. The 5500–JO2 option consists of a piggy back circuit card which is plugged into the top of the 5500–628/636 modules.

8.2.2 High Speed G.703 2.048 Mbps (5500A–J05)

The 5500–JO5 option is a factory installed option which provides the 5500A user with jitter measurement and jitter injection capability at the G.703/G.704 2.048 Mbps rate. The 5500–JO5 option consists of a piggy back circuit card which is plugged into the top of the 5500–828/836 modules.

Appendix A – Specifications

A.0 INTRODUCTION

The following paragraphs contain specifications for the Model 5500A test set. For additional information, contact your Phoenix Representative or Phoenix Customer Service at 1–800 866–8480, Ext. 255.

Table A–1. Model 5500A Specifications.

CHARACTERISTIC	SPECIFICATION
MODES OF OPERATION	
Emulation	Emulate DTE mode (for connection to DCE) Emulate DCE mode (for connection to DTE)
System Configuration	Full Duplex, Single Transmit, and Self Loop modes
Timing Modes	Synchronous, Asynchronous, and Recovered Timing
Framing Formats	D4, Unframed, ESF, and SLC®96
TRANSMITTER	
Pattern Generator	
Fixed Patterns	MARK, SPACE, ALT (1:1), LOOP–UP ("10000" repeating), and LOOP–DN ("100" repeating)
User–programmable	24 to 16,384–bit repeating pattern
Pseudorandom Patterns	63 (2^6–1), 511 (2^9–1), SYSY 511, X25 511, 2047 (2^{11}–1), Reverse 2047, 2^{15}–1, 2^{20}–1, QRW, NET55, 2^9–1A, 1:7, 3:24
Messages	FOX message (ASCII), FOX 2 (in async 5–bit baudot, 6–bit EBCDIC, 7–bit ASCII, 8–bit BCDIC; in sync 8–bit ASCII)
Message Format	Character Length – 5, 6, 7, or 8 bits (Async Timing), Parity – Odd, Even, or None, Number of Stop Bits – 1 or 2
Internal Data Rates (Synthesized)	50Hz – 500kHz @ + .1Hz increments 500kHz – 6.5MHz + 1Hz increments 6.5MHz – 13 MHz + 2Hz increments (with an accuracy of 1ppm @ 25°C; 5ppm @ 0°C to +50°C with an aging rate of 3ppm first year and 2 ppm/year thereafter.)
Data Inversion	Available for transmit and receive data
Error Insertion	Programmable from 5E–2 to 1E–9
Timing Sources	Internal Clock (see above rates), User Clock (rear panel connection), Interface Module
RECEIVER	

Table A–1. Model 5500A Specifications.(Continued)

CHARACTERISTIC	SPECIFICATION
Receiver Timing Modes	Synchronous (1 x bit rate clock received through Interface Module for bit rates from 50 bps to 13 Mbps
Data Error Analysis	
Modes	Single and Continuous
Acquiring Synchronization	MARK, SPACE, ALT, FOX, LOOP–UP, LOOP–DOWN, 0=24 + 32 = 56 BITS, SYS511, X25511 = ENTIRE PAT = 4088 BITS PSEUDORANDOMS = 24 + 32= 56 BITS
Loss of Synchronization	Adjustable – Factory setting is bit error rate of 10–1 error/bit. User may set any rate between 8.96x10–1 and 1x10–3 errors/bit
Bit Error Rate Tests	
Numeric Results Available (Interface Module Dependent)	Bit Errors, Bit Error Rate, Adjusted Bit Errors, Adjusted Bit Error Rate, Bit Count, Blocks CRC Errors, Burst Errors, CRC Error Rate, Current Bit Errors, Current Bit Error Rate, Errored Blocks, Error Free Blocks, Errored Block Rate, Frame Bit Errors, Frame Bit Error Rate, Number of Pattern Sync Losses, Power Failures, Receiver Bipolar Violations, Greater Than 15 Zeros Events, and Frame Sync Losses
Time Dependent Results (Interface Module Dependent)	Blue Alarm Seconds, Burst Errors, CRC Errored Seconds, CRC Error Free Seconds, Elapsed Days, Error Free Seconds, Errored Seconds, Errored Second Rate, Elapsed Time, Elapsed Time in Seconds, Frame Loss Seconds, Frame Bit Errored Seconds, Frame Bit Error Free Seconds, Receiver Bipolar Violation Free Seconds, Receiver Bipolar Violation Rate, Receiver Bipolar Violation Seconds, Sync Loss Seconds, Transmitter Bipolar Violation Free Seconds, Transmitter Bipolar Violation Rate, Transmitter Bipolar Violation Seconds, Time of Day, Month/Day/Year, Yellow Alarm Seconds, Greater Than 15 Zeros Seconds
Calculated Results (Interface Module Dependent)	Percent of Error Free Seconds, Percent of One's Density, Percent Frame Bit Error Free Seconds, Percent CRC Error Free Seconds, Power Failures, Wander Positive, Wander Negative, Clock Slip
Special Results	Alarms and Alarm History
G.703–815 Special Results	Transmitter Sync Loss, Transmitter Sync Loss Seconds, Receiver Sync Loss, Receiver Sync Loss Seconds, Transmitter Sync Seconds, Total Elapsed Seconds
Other Measurements	
Delay – Rising or Falling Edge Selectable	Range: 1 usec to 5 minutes, Resolution: ± 1 usec
Start/Stop Signal Sources	RTS, Receive Data, Transmit Data, SQ, DTR, DCD, DSR, and CTS
Network Loop Delay	Range: 1 usec to 5 minutes, Resolution: to ± 1 usec
Frequency	Range and Accuracy – 50Hz to 13MHz @ 1ppm
REAR PANEL CONNECTORS	
USER CLK BNC Connector	

Table A–1. Model 5500A Specifications.(Continued)

CHARACTERISTIC	SPECIFICATION
Input Signal Range	50Hz to 13MHz
Logic	1=5+.05 volts DC 0=0+.4 volts dc
Load	10 TTL loads
Outer Conductor	Ground
Inner Conductor	Signal
EXTERNAL TRIGGER	BNC Connector
RS–232	
Configuration	DCE/DTE (Switch Selectable)
Type	25–pin, D–Shell
Signal Level	1=–5V to –12V, 0=+5V to +12V
IEEE–488	
Type	IEEE–488 Standard Connector
Signal Level	1=2.5V min, 0=.5V max.
INTERFACE	50–pin Female Connector mates to Male Connector on Model 5500A Interface Modules
REAR PANEL TEST POINTS	
Signal	TXD (Transmit Data), RXD (Receive Data), TXC (Transmit Clock), RC (Receive Clock), XMIT PAT (Transmit Pattern Sync), REC PAT (Receive Pattern Sync), ERR (Bit Error Sync), REC SYNC (5500A in Sync), SP (Spare), GND (Ground)
Signal Level	1=5V+.5V, 0=0V+.4V
Pulse Width	1/2 Bit Time, minimum
REMOTE CONTROL	
Connection	RS–232 Printer/Remote Control Interface and IEEE–488 Bus Interface
Controllable Functions	All Menu Selections, Hexidecimal Keypad Entries, and Front Panel Keys
DISPLAY	
CRT Measurements	Diagonal = 5" cathode ray tube
Spherical	14.18" RAD
Deflection	70 Degrees
Resolution	Scan: 256 active pixels Frame: 768 active lines
Standard Menus Displayed	BERT Results, Help, BERT Setup, Digital Data Trap, RS–232/IEEE–4888, User Pattern, 5500A Configuration, System Options, Graph Results, Printer Setup, Store/Recall Setups, Graph Setup, G.821 Results, and Big BERT
Optional Menus Displayed	MSU Configuration, Jitter, BERT Channel, and DDS Setup
Graph Display	
Data Scale Factors	10^0, 10^1, 10^2, 10^3, 10^4, and 10^5

Table A–1. Model 5500A Specifications.(Continued)

CHARACTERISTIC	SPECIFICATION
Time Scale Factors	1 second/division, 10 seconds/division, 1 minute/division, 10 minutes/division, 60 minutes/division
Vertical Scale	0 to 100,000 units
Functions That May Be Graphed	Bit Errors, Errored Seconds, Frame Bit Errors (T1), Frame Bit Errored Seconds (T1), F–Bit Errored Seconds (T1), CRC Errors (T1), Frame Sync Losses (T1), Pattern Sync Losses, Receive BPV Seconds, > 15 Zeros Events (T1), Severely Errored Seconds (T1), Wander + (T1), Wander – (T1)
POWER REQUIREMENTS	
Voltage	100–130 Vac
Frequency	45 to 450 Hz
ENVIRONMENTAL	
Temperature	Operating 0° to +50° C; Storage –10° to +85° C
Humidity	90% Non–condensing
Weight	7–5/8H" x 18–1/2W" x 15"; weight – 21 lbs.

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Phoenix Microsystems, Inc.
991 Discovery Drive
Huntsville, AL 35806
(205) 922–1200 • 1–800 866–8480 • FAX (205) 922–1256

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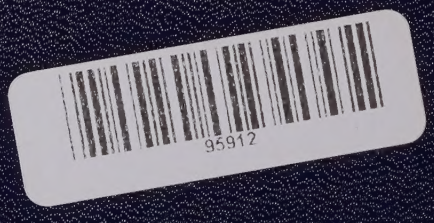
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